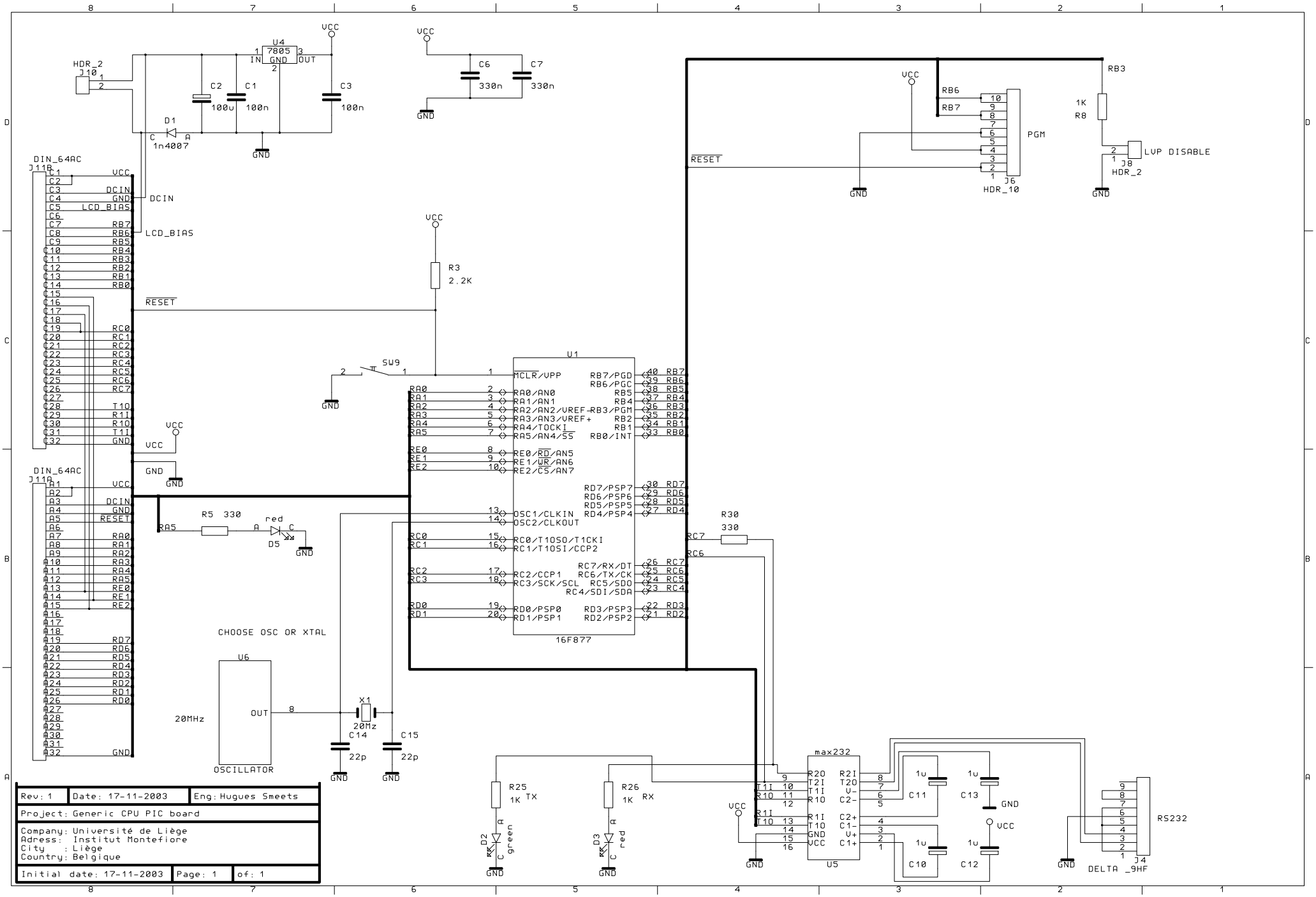
HDR_2
J10
U4
7805
IN
GND
OUT
VCC
C2
100u
C1
100n
C3
100n
D1
1n4007
C6
330n
C7
330n
DIN_64AC
J11B
DCIN
LCD_BIAS
RESET
R3
2.2K
SW9
U1
MCLR/VPP
RB7/PGD
RB6/PGC
RB5
RB4
RB3/PGM
RB2
RB1
RB0/INT
RA0/AN0
RA1/AN1
RA2/AN2/VREF-
RA3/AN3/VREF+
RA4/T0CKI
RA5/AN4/SS
RE0/RD/AN5
RE1/WR/AN6
RE2/CS/AN7
RD7/PSP7
RD6/PSP6
RD5/PSP5
RD4/PSP4
OSC1/CLKIN
OSC2/CLKOUT
RC0/T1OSO/T1CKI
RC1/T1OSI/CCP2
RC2/CCP1
RC3/SCK/SCL
RC7/RX/DT
RC6/TX/CK
RC5/SDO
RC4/SDI/SDA
RD0/PSP0
RD1/PSP1
RD3/PSP3
RD2/PSP2
16F877
DIN_64AC
J11A
R5 330
red
D5
R30
330
CHOOSE OSC OR XTAL
U6
OUT
20MHz
X1
20Mz
C14
22p
C15
22p
OSCILLATOR
R25
1K
TX
R26
1K
RX
D2
green
D3
red
max232
R2O
R2I
T2I
T2O
T1I
V-
R1O
C2-
R1I
C2+
T1O
C1-
GND
V+
VCC
C1+
U5
C11
C13
C10
C12
1u
RB6
RB7
RB3
1K
R8
PGM
J6
HDR_10
LVP DISABLE
J8
HDR_2
RS232
J4
DELTA _9HF
Rev: 1
Date: 17-11-2003
Eng: Hugues Smeets
Project: Generic CPU PIC board
Company: Université de Liège
Adress: Institut Montefiore
City : Liège
Country: Belgique
Initial date: 17-11-2003
Page: 1
of: 1