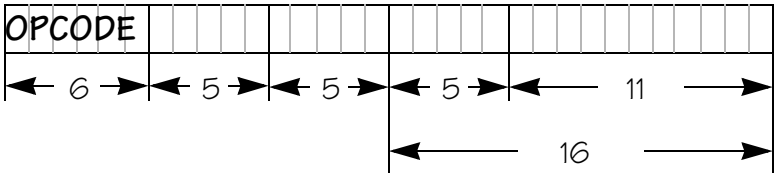
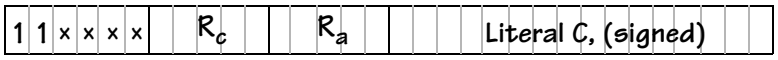
BETA Architecture for 6.004: Instruction Formats - 10/97 SAW



Operate class: $R_c \leftarrow \langle R_a \rangle$ op $\langle R_b \rangle$



Operate class: $R_c \leftarrow \langle R_a \rangle$ op C

Opcodes, both formats:

ADD	SUB	MUL*	DIV*	*optional
CMPEQ	CMPLE	CMPLT		
AND	OR	XOR		
SHL	SHR	SRA		

LD: $R_c \leftarrow Mem[\langle R_a \rangle + C]$

ST: $Mem[\langle R_a \rangle + C] \leftarrow \langle Rc \rangle$

JMP: $R_c \leftarrow \langle PC \rangle + 4$; $PC \leftarrow \langle R_a \rangle$

BEQ: $R_c \leftarrow \langle PC \rangle + 4$; if $\langle Ra \rangle = 0$ then $PC \leftarrow \langle PC \rangle + 4 + (C << 2)$

BNE: $R_c \leftarrow \langle PC \rangle + 4$; if $\langle Ra \rangle \neq 0$ then $PC \leftarrow \langle PC \rangle + 4 + (C << 2)$

LDR: $R_c \leftarrow \langle \langle PC \rangle + 4 + (C << 2) \rangle$

Opcode Map: (* optional)

	000	001	010	011	100	101	110	111
000								
001								
010								
011	LD	ST		JMP		BEQ	BNE	LDR
100	ADD	SUB	MUL*	DIV*	CMPEQ	CMPLT	CMPLE	
101	AND	OR	XOR		SHL	SHR	SRA	
110	ADDC	SUBC	MULC*	DIVC*	CMPEQC	CMPLTC	CMPLEC	
111	ANDC	ORC	XORC		SHLC	SHRC	SRAC	