DATA SHEET

FAMILY SPECIFICATIONS
HCMOS family characteristics

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Philips
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HCMOS family characteristics

FAMILY SPECIFICATIONS

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the “HC-types”, will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account
(see also *“HANDLING PRECAUTIONS”*).

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	–40		+85	–40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	–40		+125	–40		+125	°C	
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

Note

1. For analog switches, e.g. “4016”, “4051 series”, “4351 series”, “4066” and “4067”, the specified maximum operating supply voltage is 10 V.

RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	–40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	–40		+125	°C	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current				for $-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V
	standard outputs		25	mA	
	bus driver outputs		35	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with:				
	standard outputs		50	mA	
	bus driver outputs		70	mA	
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: –40 to +125 °C 74HC/HCT/HCU
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

Note

1. For analog switches, e.g. “4016”, “4051 series”, “4351 series”, “4066” and “4067”, the specified maximum operating supply voltage is 11 V.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA $-I_O$ = 7.8 mA
V_{OL}	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage standard outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
V_{OL}	LOW level output voltage bus driver outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 6.0 mA I_O = 7.8 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current											
	SSI			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	I_O = 0
	flip-flops			4.0		40.0		80.0		6.0		I_O = 0
	MSI			8.0		80.0		160.0		6.0		I_O = 0
	LSI			50.0		500		1000		6.0		I_O = 0

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage standard outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA
V_{OL}	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage standard outputs		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
V_{OL}	LOW level output voltage bus driver outputs		0.16	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
I_{CC}	quiescent supply current											
	SSI			2.0		20.0		40.0	μA	5.5	V_{CC} or GND	I_O = 0
	flip-flops			4.0		40.0		80.0		5.5		I_O = 0
	MSI			8.0		80.0		160.0		5.5		I_O = 0
	LSI			50.0		500		1000		5.5		I_O = 0

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; I_O = 0

Note

1. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCU										
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 µA $-I_O$ = 20 µA $-I_O$ = 20 µA
V_{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{CC} or GND	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 µA I_O = 20 µA I_O = 20 µA
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{CC} or GND	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	µA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current SSI			2.0		20.0		40.0	µA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs		19	75		95		110	ns	2.0	Figs 3 and 4
			7	15		19		22		4.5	
			6	13		16		19		6.0	
t_{THL}/ t_{TLH}	output transition time bus driver outputs		14	60		75		90	ns	2.0	Figs 3 and 4
			5	12		15		18		4.5	
			4	10		13		15		6.0	

AC CHARACTERISTICS FOR 74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCU								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time		19	75		95		110	ns	2.0	Fig.1
			7	15		19		22		4.5	
			6	13		16		19		6.0	

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs		7	15		19		22	ns	4.5	Figs 8 and 9
t_{THL}/ t_{TLH}	output transition time bus driver outputs		5	12		15		18	ns	4.5	Figs 8 and 9

HCU TYPES

AC waveforms 74HCU

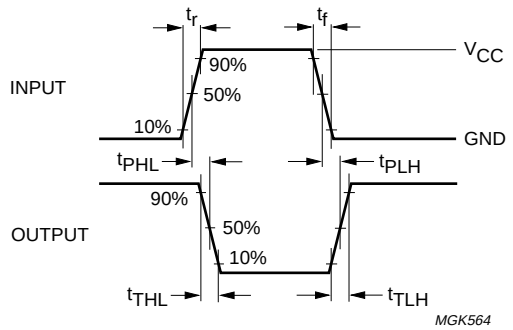
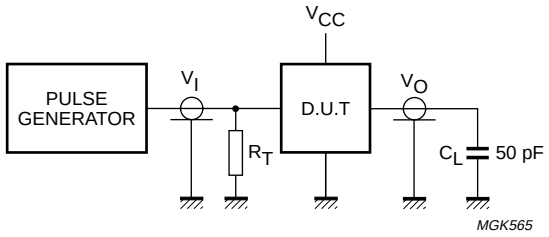


Fig.1 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

Test circuit for 74HCU



C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.2 Test circuit.

HC TYPES

AC waveforms 74HC

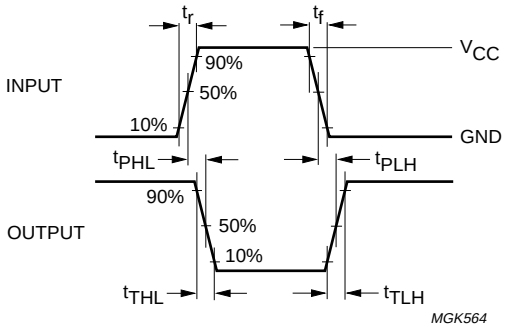
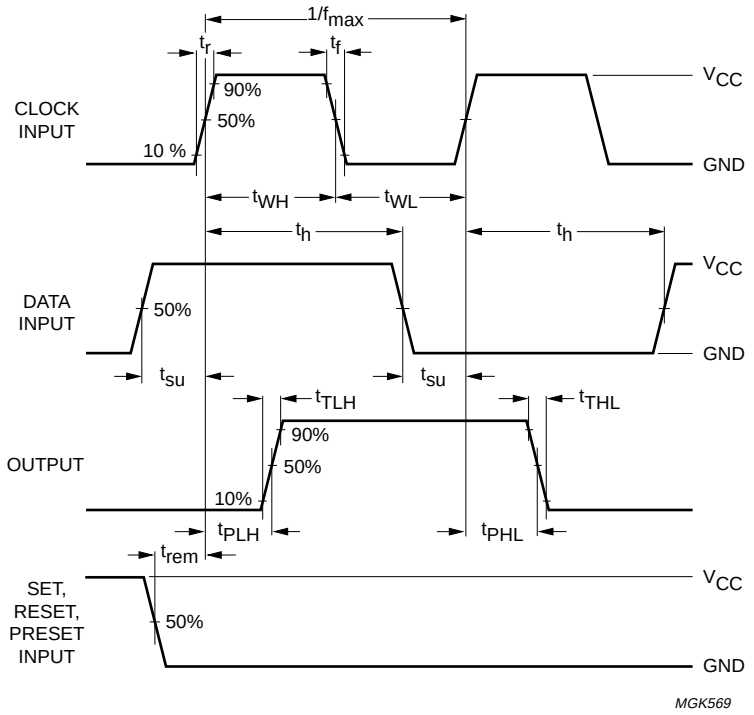


Fig.3 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC waveforms 74HC

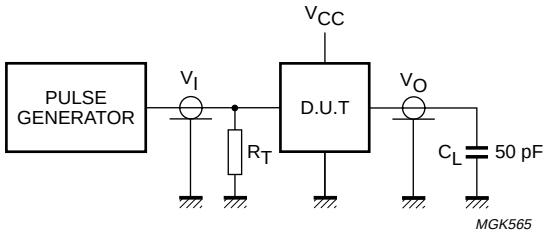


(1) In Fig.4 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

(2) For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Fig.4 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Test circuit for 74HC



C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.5 Test circuit.

AC waveforms 74HC (continued)

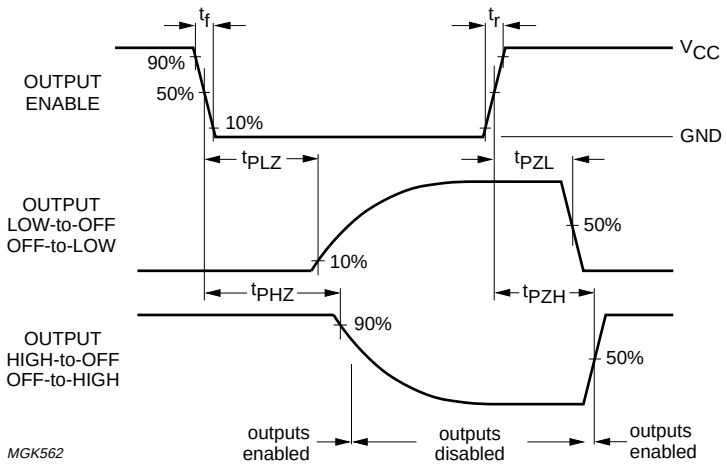
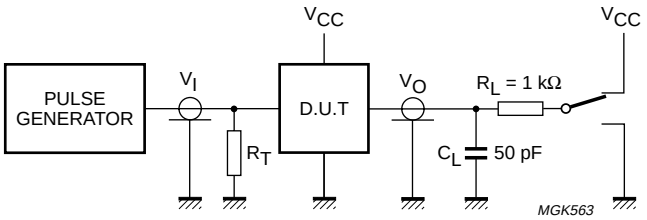


Fig.6 Propagation delays of 3-state outputs.

Test circuit for 74HC



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note

1. For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Test circuit for 3-state outputs.

HCT TYPES

AC waveforms 74HCT

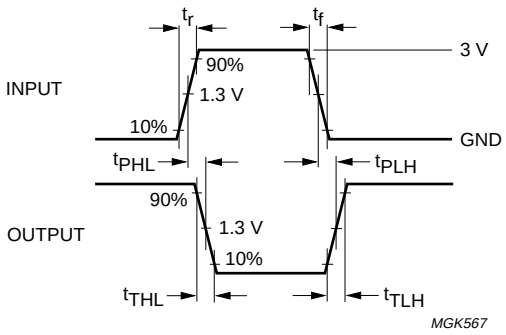
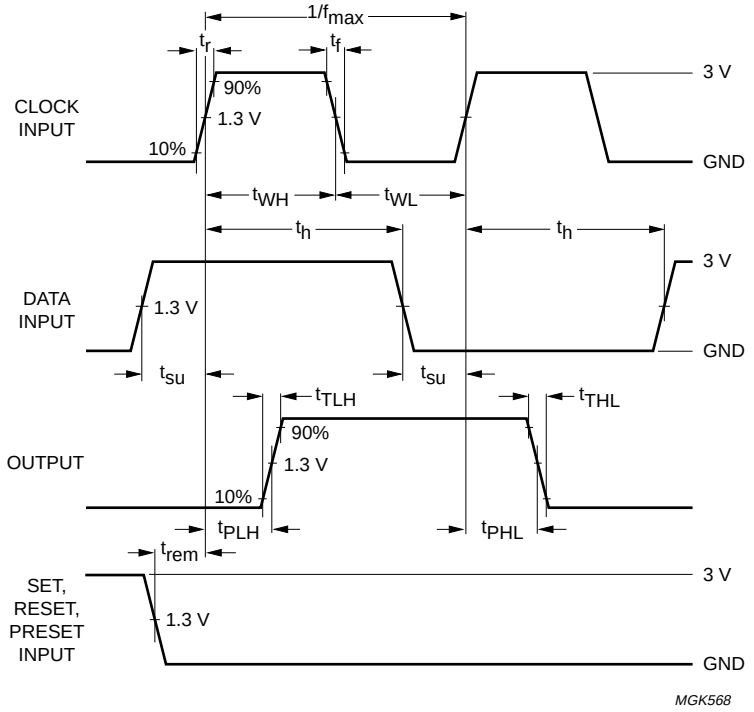


Fig.8 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC waveforms 74HCT

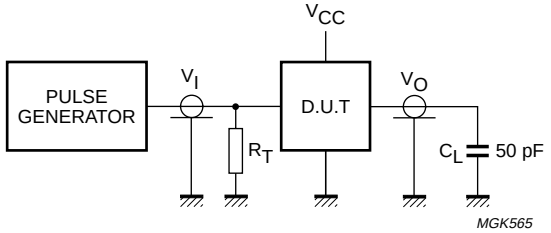


(1) In Fig.9 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

(2) For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Fig.9 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Test circuit for 74HCT



C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Test circuit.

AC waveforms 74HCT (continued)

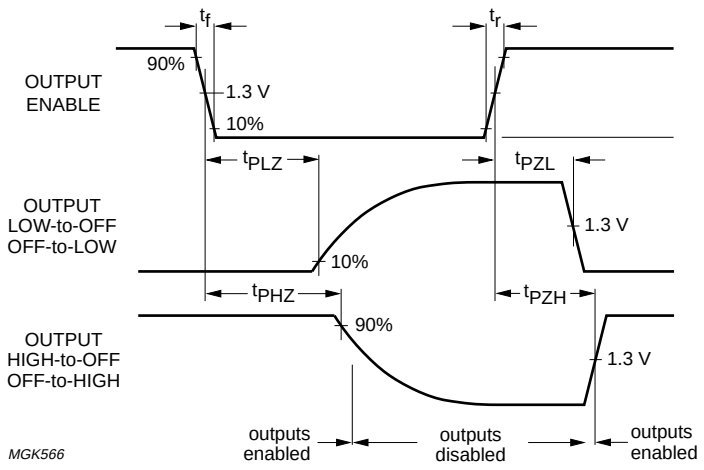
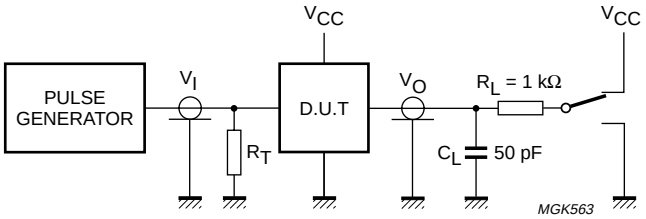


Fig.11 Propagation delays of 3-state outputs.

Test circuit for 74HCT



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note

1. For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.12 Test circuit for 3-state outputs.

DATA SHEET SPECIFICATION GUIDE

INTRODUCTION

The 74HCMOS data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for the longest data path through the device with a 15 pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_r and t_f.

LOGIC SYMBOLS

Two logic symbols are given for each device - the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEC Logic Symbol as developed by the IEC (International Electrotechnical Commission).

The IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic.
Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) which supersedes Publication 117-15, published in 1972.

RATINGS

The “RATINGS” table (Limiting values in accordance with the Absolute Maximum System - IEC134) lists the maximum limits to which the device can be subjected without damage. This doesn’t imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life won’t have been shortened.

The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V.

RECOMMENDED OPERATING CONDITIONS

The “RECOMMENDED OPERATING CONDITIONS” table lists the operating ambient temperature and the conditions under which the limits in the “DC CHARACTERISTICS” and “AC CHARACTERISTICS” tables will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC CHARACTERISTICS tables.

DC CHARACTERISTICS

The “DC CHARACTERISTICS” table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} can be tested by the user. If V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the “DC CHARACTERISTICS” table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a “function-table exercizer” mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 metre. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any HCMOS device type; instead, use input voltages of V_{CC} (for the HIGH state) and 0 V (for the LOW state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because V_{ILmax} is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic LOW. However, typically a **higher** V_{IL} will also be recognized as a logic LOW. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

For 74HCMOS, unlike TTL, no output HIGH short-circuit current is specified. The use of this current, for example, to calculate propagation delays with capacitive loads, is covered by the HCMOS graphs showing the output drive capability and those showing the dependence of propagation delay on load capacitance.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors. It is measured with the inputs at V_{CC} or GND and is typically a few nA.

AC CHARACTERISTICS

The “AC CHARACTERISTICS” table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveforms section.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground-plane) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 6 ns, a signal swing of 0 V to V_{CC} for 74HC and 0 V to 3 V for 74HCT; a 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as set-up time, hold time and removal time. f_{max} is also tested with 6 ns input rise and fall times, with a 50% duty factor, but for typical f_{max} as high as 60 MHz, there are no constraints on rise and fall times.

DEFINITIONS OF SYMBOLS AND TERMS USED IN HCMOS DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{CC}	Quiescent power supply current; the current flowing into the V_{CC} supply terminal.
ΔI_{CC}	Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.
I_{GND}	Quiescent power supply current; the current flowing into the GND terminal.
I_I	Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.
I_{IK}	Input diode current; the current flowing into a device at a specified input voltage.
I_O	Output source or sink current: the current flowing into a device at a specified output voltage.
I_{OK}	Output diode current; the current flowing into a device at a specified output voltage.
I_{OZ}	OFF-state output current; the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.
I_S	Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V**.**

GND	Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.
V_{CC}	Supply voltage; the most positive potential on the device.
V_{EE}	Supply voltage; one of two (GND and V_{EE}) negative power supplies.
V_H	Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative-going input signal.
V_{IH}	HIGH level input voltage; the range of input voltages that represents a logic HIGH level in the system.
V_{IL}	LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.
V_{OH}	HIGH level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.
V_{OL}	LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.
V_{T+}	Trigger threshold voltage; positive-going signal.
V_{T-}	Trigger threshold voltage; negative-going signal.

Analog terms

R_{ON}	ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.
ΔR_{ON}	ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I	Input capacitance; the capacitance measured at a terminal connected to an input of a device.
$C_{I/O}$	Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).
C_L	Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.
C_{PD}	Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.
C_S	Switch capacitance; the capacitance of a terminal to a switch of an analog device.

AC switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.

t_h Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_r, t_f Clock input rise and fall times; 10% and 90% values.

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V points for the 74HCT devices, with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V point for the 74HCT devices, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC and 74HCU devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).

t_{PLZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (V_{OL}) to a high impedance OFF-state (Z).

t_{PZH} 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (V_{OH}).

t_{PZL} 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (V_{OL}).

t_{rem} Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74HC devices and the 1.3 V points for the 74HCT devices on both input voltage waveforms.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL}	Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to-LOW.
t_{THL}	Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to-HIGH.
t_W	Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74HC and 74HCU devices and at the 1.3 V points for 74HCT devices.

Package information

Supersedes data of 1999 Sep 22
File under Integrated Circuits, IC06

2001 Nov 02

Philips
Semiconductors

PHILIPS

Package information

PACKAGE INFORMATION

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HCU04	27-1	108-1	337-1	402-1	14
74HCTU04	27-1	108-1			14
74HC00	27-1	108-1	337-1	402-1	14
74HCT00	27-1	108-1	337-1	402-1	14
74HC02	27-1	108-1	337-1	402-1	14
74HCT02	27-1	108-1	337-1	402-1	14
74HC03	27-1	108-1	337-1	402-1	14
74HCT03	27-1	108-1	337-1	402-1	14
74HC04	27-1	108-1	337-1	402-1	14
74HCT04	27-1	108-1	337-1	402-1	14
74HC08	27-1	108-1	337-1	402-1	14
74HCT08	27-1	108-1	337-1	402-1	14
74HC10	27-1	108-1	337-1	402-1	14
74HCT10	27-1	108-1	337-1	402-1	14
74HC42	38-1	109-1			16
74HCT42	38-1	109-1			16
74HC107	27-1	108-1	337-1	402-1	14
74HCT107	27-1	108-1	337-1	402-1	14
74HC109	38-1	109-1			16
74HCT109	38-1	109-1	338-1		16
74HC11	27-1	108-1	337-1	402-1	14
74HCT11	27-1	108-1	337-1	402-1	14
74HC112	38-1	109-1	338-1	403-1	16
74HCT112	38-1	109-1	338-1	403-1	16
74HC123	38-1	109-1	338-1	403-1	16
74HCT123	38-1	109-1	338-1	403-1	16
74HC125	27-1	108-1	337-1	402-1	14
74HCT125	27-1	108-1	337-1	402-1	14
74HC126	27-1	108-1	337-1	402-1	14
74HCT126	27-1	108-1	337-1	402-1	14
74HC1284		163-1	339-1	360-1	20
74HCT1284		163-1	339-1	360-1	20
74HC132	27-1	108-1	337-1	402-1	14
74HCT132	27-1	108-1	337-1	402-1	14
74HC133	38-1	109-1			16
74HCT133	38-1	109-1			16
74HC137	38-1	109-1	338-1		16
74HCT137	38-1	109-1			16
74HC138	38-1	109-1	338-1	403-1	16
74HCT138	38-1	109-1	338-1	403-1	16

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HC139	38-1	109-1	338-1	403-1	16
74HCT139	38-1	109-1	338-1	403-1	16
74HC14	27-1	108-1	337-1	402-1	14
74HCT14	27-1	108-1	337-1	402-1	14
74HC147	38-1	109-1	338-1		16
74HCT147	38-1	109-1	338-1		16
74HC151	38-1	109-1	338-1	403-1	16
74HCT151	38-1	109-1	338-1	403-1	16
74HC153	38-1	109-1	338-1	403-1	16
74HCT153	38-1	109-1	338-1	403-1	16
74HC154	101-1	137-1	340-1	355-1	24
74HCT154	101-1	137-1	340-1	355-1	24
74HC157	38-1	109-1	338-1	403-1	16
74HCT157	38-1	109-1	338-1	403-1	16
74HC158	38-1	109-1			16
74HCT158	38-1	109-1			16
74HC160	38-1	109-1	338-1		16
74HCT160	38-1	109-1			16
74HC161	38-1	109-1	338-1	403-1	16
74HCT161	38-1	109-1	338-1	403-1	16
74HC162	38-1	109-1			16
74HCT162	38-1	109-1			16
74HC163	38-1	109-1	338-1	403-1	16
74HCT163	38-1	109-1	338-1	403-1	16
74HC164	27-1	108-1	337-1	402-1	14
74HCT164	27-1	108-1	337-1	402-1	14
74HC165	38-1	109-1	338-1	403-1	16
74HCT165	38-1	109-1	338-1	403-1	16
74HC166	38-1	109-1	338-1	403-1	16
74HCT166	38-1	109-1	338-1		16
74HC173	38-1	109-1	338-1	403-1	16
74HCT173	38-1	109-1	338-1		16
74HC174	38-1	109-1	338-1	403-1	16
74HCT174	38-1	109-1	338-1	403-1	16
74HC175	38-1	109-1	338-1	403-1	16
74HCT175	38-1	109-1	338-1	403-1	16
74HC181	101-1	137-1			24
74HCT181	101-1	137-1			24
74HC182	38-1	109-1			16
74HCT182	38-1	109-1			16

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HC190	38-1	109-1			16
74HCT190	38-1	109-1			16
74HC191	38-1	109-1	338-1	403-1	16
74HCT191	38-1	109-1			16
74HC192	38-1	109-1	338-1		16
74HCT192	38-1	109-1			16
74HC193	38-1	109-1	338-1	403-1	16
74HCT193	38-1	109-1	338-1		16
74HC194	38-1	109-1	338-1		16
74HCT194	38-1	109-1	338-1		16
74HC195	38-1	109-1	338-1		16
74HCT195	38-1	109-1	338-1		16
74HC20	27-1	108-1	337-1	402-1	14
74HCT20	27-1	108-1	337-1		14
74HC21	27-1	108-1	337-1		14
74HCT21	27-1	108-1	337-1		14
74HC221	38-1	109-1	338-1		16
74HCT221	38-1	109-1	338-1		16
74HC237	38-1	109-1	338-1		16
74HCT237	38-1	109-1	338-1		16
74HC238	38-1	109-1	338-1	403-1	16
74HCT238	38-1	109-1	338-1	403-1	16
74HC240	146-1	163-1	339-1	360-1	20
74HCT240	146-1	163-1	339-1	360-1	20
74HC241	146-1	163-1	339-1	360-1	20
74HCT241	146-1	163-1	339-1	360-1	20
74HC242	27-1	108-1	337-1		14
74HCT242	27-1	108-1			14
74HC243	27-1	108-1	337-1		14
74HCT243	27-1	108-1	337-1		14
74HC244	146-1	163-1	339-1	360-1	20
74HCT244	146-1	163-1	339-1	360-1	20
74HC245	146-1	163-1	339-1	360-1	20
74HCT245	146-1	163-1	339-1	360-1	20
74HC251	38-1	109-1	338-1	403-1	16
74HCT251	38-1	109-1	338-1	403-1	16
74HC253	38-1	109-1	338-1		16
74HCT253	38-1	109-1	338-1		16
74HC257	38-1	109-1	338-1	403-1	16
74HCT257	38-1	109-1	338-1	403-1	16

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HC258	38-1	109-1	338-1		16
74HCT258	38-1	109-1			16
74HC259	38-1	109-1	338-1	403-1	16
74HCT259	38-1	109-1	338-1	403-1	16
74HC27	27-1	108-1	337-1	402-1	14
74HCT27	27-1	108-1	337-1	402-1	14
74HC273	146-1	163-1	339-1	360-1	20
74HCT273	146-1	163-1	339-1	360-1	20
74HC280	27-1	108-1	337-1	402-1	14
74HCT280	27-1	108-1		402-1	14
74HC283	38-1	109-1	338-1	403-1	16
74HCT283	38-1	109-1	338-1	403-1	16
74HC297	38-1	109-1			16
74HCT297	38-1	109-1			16
74HC299	146-1	163-1	339-1		20
74HCT299	146-1	163-1	339-1		20
74HC30	27-1	108-1	337-1	402-1	14
74HCT30	27-1	108-1	337-1	402-1	14
74HC32	27-1	108-1	337-1	402-1	14
74HCT32	27-1	108-1	337-1	402-1	14
74HC354	146-1	163-1			20
74HCT354	146-1	163-1			20
74HC356	146-1	163-1			20
74HCT356	146-1	163-1			20
74HC365	38-1	109-1	338-1	403-1	16
74HCT365	38-1	109-1	338-1		16
74HC366	38-1	109-1			16
74HCT366	38-1	109-1	338-1		16
74HC367	38-1	109-1	338-1	403-1	16
74HCT367	38-1	109-1	338-1	403-1	16
74HC368	38-1	109-1	338-1		16
74HCT368	38-1	109-1	338-1	403-1	16
74HC373	146-1	163-1	339-1	360-1	20
74HCT373	146-1	163-1	339-1	360-1	20
74HCT374	146-1	163-1	339-1	360-1	20
74HC374	146-1	163-1	339-1	360-1	20
74HCT377	146-1	163-1	339-1	360-1	20
74HC377	146-1	163-1	339-1	360-1	20
74HC390	38-1	109-1	338-1	403-1	16
74HCT390	38-1	109-1	338-1		16

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HC393	27-1	108-1	337-1	402-1	14
74HCT393	27-1	108-1	337-1	402-1	14
74HC4002	27-1	108-1	337-1	402-1	14
74HCT4002	27-1	108-1	337-1		14
74HC4015	38-1	109-1			16
74HCT4015	38-1	109-1			16
74HC4016	38-1	109-1			16
74HCT4016	38-1	109-1			16
74HC4017	38-1	109-1			16
74HCT4017	38-1	109-1			16
74HC40102	38-1	109-1			16
74HCT40102	38-1	109-1			16
74HC40103	38-1	109-1	338-1	403-1	16
74HCT40103	38-1	109-1	338-1		16
74HC40104	38-1	109-1			16
74HCT40104	38-1	109-1			16
74HC40105	38-1	109-1	338-1	403-1	16
74HCT40105	38-1	109-1	338-1		16
74HC4020	38-1	109-1	338-1	403-1	16
74HCT4020	38-1	109-1	338-1	403-1	16
74HC4024	27-1	108-1	337-1		14
74HCT4024	27-1	108-1			14
74HC4040	38-1	109-1	338-1	403-1	16
74HCT4040	27-1	109-1			16
74HC4046A	38-1	109-1	338-1	403-1	16
74HCT4046A	38-1	109-1	338-1		16
74HC4049	38-1	109-1			16
74HCT4049	38-1	109-1			16
74HC4050	38-1	109-1	338-1	403-1	16
74HCT4050	38-1	109-1			16
74HC4051	38-1	109-1	338-1	403-1	16
74HCT4051	38-1	109-1	338-1		16
74HC4052	38-1	109-1	338-1	403-1	16
74HCT4052	38-1	109-1	338-1		16
74HC4053	38-1	109-1	338-1	403-1	16
74HCT4053	38-1	109-1	338-1	403-1	16
74HC4059	101-1	137-1			24
74HCT4059	101-1	137-1			24
74HC4060	38-1	109-1	338-1	403-1	16
74HCT4060	38-1	109-1	338-1		16

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HCT4066	27-1	108-1	337-1	402-1	14
74HC4066	27-1	108-1	337-1	402-1	14
74HC4067	101-1	137-1	340-1	355-1	24
74HCT4067	101-1	137-1	340-1	355-1	24
74HC4075	27-1	108-1	337-1		14
74HCT4075	27-1	108-1	337-1	402-1	14
74HC4094	38-1	109-1	338-1		16
74HCT4094	38-1	109-1	338-1		16
74HC423	38-1	109-1			16
74HCT423	38-1	109-1			16
74HC4316	38-1	109-1	338-1	403-1	16
74HCT4316	38-1	109-1	338-1	403-1	16
74HC4351	146-1	163-1	339-1		20
74HCT4351	146-1	163-1	339-1		20
74HC4352	146-1	163-1			20
74HCT4352	146-1	163-1			20
74HC4510	38-1	109-1			16
74HCT4510	38-1	109-1			16
74HC4511	38-1	109-1			16
74HCT4511	38-1	109-1			16
74HC4514	101-1	137-1	340-1		24
74HCT4514	101-1	137-1	340-1		24
74HC4515	101-1	137-1			24
74HCT4515	101-1	137-1			24
74HC4516	38-1	109-1			16
74HCT4516	38-1	109-1			16
74HC4518	38-1	109-1			16
74HCT4518	38-1	109-1			16
74HC4520	38-1	109-1	338-1	403-1	16
74HCT4520	38-1	109-1	338-1		16
74HC4538	38-1	109-1	338-1	403-1	16
74HCT4538	38-1	109-1	338-1	403-1	16
74HC4543	38-1	109-1			16
74HCT4543	38-1	109-1			16
74HC533	146-1	163-1			20
74HCT533	146-1	163-1			20
74HC534	146-1	163-1			20
74HCT534	146-1	163-1			20
74HC540	146-1	163-1	339-1		20
74HCT540	146-1	163-1	339-1		20

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HC541	146-1	163-1	339-1	360-1	20
74HCT541	146-1	163-1	339-1	360-1	20
74HC5555	38-1	109-1			16
74HCT5555	38-1	109-1			16
74HC563	146-1	163-1			20
74HCT563	146-1	163-1	339-1		20
74HC564	146-1	163-1			20
74HCT564	146-1	163-1			20
74HC573	146-1	163-1	339-1	360-1	20
74HCT573	146-1	163-1	339-1	360-1	20
74HC574	146-1	163-1	339-1	360-1	20
74HCT574	146-1	163-1	339-1	360-1	20
74HC58	27-1	108-1	337-1		14
74HC583	38-1	109-1			16
74HCT583	38-1	109-1			16
74HC594	38-1	109-1	338-1		16
74HCT594	38-1	109-1			16
74HC595	38-1	109-1	338-1	403-1	16
74HCT595	38-1	109-1	338-1	403-1	16
74HC597	38-1	109-1	338-1	403-1	16
74HCT597	38-1	109-1	338-1		16
74HC6323A		96-1			8
74HCT6323A		96-1			8
74HC640	146-1	163-1	339-1		20
74HCT640	146-1	163-1	339-1		20
74HC643	146-1	163-1			20
74HCT643	146-1	163-1			20
74HC646	101-1	137-1	340-1		24
74HCT646	101-1	137-1	340-1		24
74HC648	101-1	137-1			24
74HCT648	101-1	137-1			24
74HC652	101-1	137-1			24
74HCT652	101-1	137-1			24
74HC670	38-1	109-1	338-1		16
74HCT670	38-1	109-1	338-1		16
74HC688	146-1	163-1	339-1	360-1	20
74HCT688	146-1	163-1	339-1	360-1	20
74HC7014	27-1	108-1			14
74HCT7014	27-1	108-1			14
74HC7030	117-1	136-1			28

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HCT7030	117-1	136-1			28
74HC7046A	38-1	109-1	338-1		16
74HCT7046A	38-1	109-1			16
74HC7080	146-1	163-1			20
74HCT7080	146-1	163-1			20
74HC7132	27-1	108-1			14
74HCT7132	27-1	108-1			14
74HC7245	146-1	163-1			20
74HCT7245	146-1	163-1			20
74HC7266	27-1	108-1	337-1		14
74HCT7266	27-1	108-1			14
74HC73	27-1	108-1			14
74HCT73	27-1	108-1	337-1		14
74HC74	27-1	108-1			14
74HCT74	27-1	108-1	337-1	402-1	14
74HC7403	38-1	109-1			16
74HCT7403	38-1	109-1			16
74HC7404	102-1	163-1			18/20
74HCT7404	102-1	163-1			18/20
74HC75	38-1	109-1	338-1	403-1	16
74HCT75	38-1	109-1	338-1		16
74HC7540	146-1	163-1	339-1		20
74HCT7540	146-1	163-1			20
74HC7541	146-1	163-1	339-1		20
74HCT7541	146-1	163-1			20
74HC7597	38-1	109-1			16
74HCT7597	38-1	109-1			16
74HC7731	38-1	109-1			16
74HCT7731	38-1	109-1			16
74HC85	38-1	109-1	338-1	403-1	16
74HCT85	38-1	109-1	338-1		16
74HC86	27-1	108-1	337-1	402-1	14
74HCT86	27-1	108-1	337-1	402-1	14
74HC9014	146-1	163-1			20
74HCT9014	146-1	163-1			20
74HC9015	146-1	163-1		360-1	20
74HCT9015	146-1	163-1			20
74HC9046A	38-1	109-1			16
74HCT9046A	38-1	109-1		403-1	16
74HC9114	146-1	163-1			20

Package information

PART NO	DIP (N)	SO (D)	SSOP (DB)	TSSOP (PW)	PIN COUNT
74HCT9114	146-1	163-1			20
74HC9115	146-1	163-1			20
74HCT9115	146-1	163-1			20
74HC93	27-1	108-1	337-1		14
74HCT93	27-1	108-1			14
74HC9323A		96-1			8
74HCT9323A		96-1			8

74HC/T Cross Reference Card

On Semiconductor and TI to Philips

FUNCTION	DESCRIPTION	NO. PINS	PHILIPS	ON SEMI	TI
74HC/T00	QUAD 2-INPUT NAND GATE	14	A		A
74HC/T02	QUAD 2-INPUT NOR GATE	14	A		A
74HC/T03	QUAD 2-INPUT NAND GATE (OC)	14	A		A
74HC/T04	HEX INVERTER	14	A		A
74HCU04	HEX INVERTER (UNBUFFERED)	14	A	A	A
74HC/T08	QUAD 2-INPUT AND GATE	14	A		A
74HC/T10	TRIPLE 3-INPUT NAND GATE	14	A	A	A
74HC/T107	DUAL J-K NEG EDGE F/F/ RES	14	A	A	A
74HC/T109	DUAL J-K POS EDGE F/F/SET, RES	16	A	A	A
74HC/T11	TRIPLE 3-INPUT AND GATE	14	A	A	A
74HC/T112	DUAL J-K NEG EDGE F/F/RESET	16	A	A	A
74HC/T123	DUAL RETRIG MONOSTBL MULTIVIBR	16	A		A
74HC/T125	QUAD BUFFER/DRVR 3-S	14	A		A
74HC/T126	QUAD BUFFER/DRVR 3-S	14	A		A
74HC/T132	QUAD 2-INPUT NAND SCHMITT TRIG	14	A		A
74HC133	13 INPUT NAND GATE	16	A	A	
74HC/T137	3 TO 8 LINE DECODER/DEMUX	16	A	A	A
74HC/T138	3-TO-8 LINE DECODER/DEMUX, INV	16	A		A
74HC/T139	DUAL 2-TO-4 LINE DECODER/DEMUX	16	A		A
74HC/T14	HEX INVERTING SCHMITT TRIGGER	14	A		A
74HC/T147	10-TO-4 LINE PRIORITY ENCODER	16	A	A	A
74HC/T151	8-INPUT MULTIPLEXER	16	A	A	A
74HC/T153	DUAL 4-INPUT MULTIPLEXER	16	A	A	A
74HC/T154	4-TO-16 LINE DECODER/DEMUX	24	A	A	A
74HC/T157	QUAD 2-INPUT MULTIPLEXER	16	A		A
74HC/T158	QUAD 2-INPUT MULTIPLEXER, INV	16	A	A	A
74HC/T161	SYNCH 4-BIT BINARY CNTR,ASYNC RES	16	A		A
74HC/T163	SYNC. 4-BIT BINARY CNTR, SYNC RES	16	A		A
74HC/T164	8 BIT SERIAL-IN/PARALLEL OUT REGISTER	14	A	A	A
74HC/T165	8 BIT PARALLEL-IN SERIAL-OUT REGISTER	16	A	A	A
74HC/T166	8-BIT SI-PO SHIFT REGISTER	16	A		A
74HC/T173	DUAL D-TYPE F/F, POS EDGE TRIG	16	A	A	A
74HC174	HEX D-TYPE F/F, POS EDGE TRIG	16	A		A
74HC/T175	QUAD D-TYPE F/F, POS EDGE TRIG	16	A	A	A
74HC/T191	SYNC BINARY UP/DON COUNTER	16	A		A
74HC192	SYNC DECADE UP/DON COUNTER	16	A		A
74HC/T193	SYNCH 4-BIT BINARY UP/DON CNTR	16	A		A
74HC/T194	4-BIT BIDIRECTIONAL SHIFT REG	16	A	A	A
74HC195	4-BIT PARALLEL-ACCESS SHIFT REG	16	A	A	A
74HC/T20	DUAL 4-INPUT NAND GATE	14	A	A	A
74HC/T21	DUAL 4-INPUT AND GATE	14	A		A
74HC/T221	DUAL MONOSTABLE MULTIVIBRATOR	16	A		A
74HC/T237	3-TO-8 LINE DECOD/DEMUX/AD LATCH	16	A	A	A
74HC/T238	3-TO-8 LINE DECODER/DEMUX	16	A		A
74HC/T240	OCT BUF/LINE DRVR, INV 3-S	20	A		A
74HC/T241	OCT LINE DRVR, 3-S	20	A		A
74HC/T242	QUAD BUS XCVR, INV 3-S	14	A	A	
74HC/T243	QUAD BUS TRANSCEIVER, 3-S	14	A		A
74HC/T244	OCT LINE DRVR, 3-S	20	A		A
74HC/T245	OCTAL BUS TRANSCEIVER 3-S	20	A		A
74HC/T251	8-INPUT MUX, 3-STATE	16	A	A	A
74HC/T253	DUAL 4-INPUT MULTIPLEXER, 3-S	16	A	A	A
74HC/T257	QUAD 2-INPUT MULTIPLEXER, 3-S	16	A	A	A
74HCT258	QUAD 2-INPUT MULTIPLEXER; 3-S; INV.	16	A		A
74HC/T259	8-BIT ADDRESSABLE LATCH	16	A	A	A
74HC/T27	TRIPLE 3-INPUT NOR GATE	14	A	A	A
74HC/T273	OCT D-TYPE F/F/POS EDGE TRIG	20	A		A
74HC/T280	9-BIT ODD/EVEN PAR GEN/CHECKER	14	A	A	A
74HC/T283	4-BIT FULL ADDER/FAST CARRY	16	A		A
74HC/T297	DIG PHASE LOCKED LOOP FILTER	16	A		A
74HC/T299	8-BIT UNIVERSAL SHIFT REG 3-S	20	A	A	A
74HC/T30	8-INPUT NAND GATE	14	A	A	A
74HC/T32	QUAD 2-INPUT OR GATE	14	A		A

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PHILIPS

74HC/T Cross Reference Card

FUNCTION	DESCRIPTION	NO. PINS	PHILIPS	ON SEMI	TI
74HC/T354	8 INPUT MUX/REGISTER	20	A	A	A
74HC/T365	8-BIT MULTIPLEXER/REG,3-STATE	16	A	A	A
74HC/T366	HEX BUFFER/LINE DRVR, INV 3-S	16	A	A	A
74HC/T367	HEX BUFFER/LINE DRVR, 3-S	16	A	A	A
74HC/T368	HEX BUFFER/LINE DRVR, INV 3-S	16	A	A	A
74HC/T373	OCT D-TYPE TRANSP LATCH, 3-S	20	A		A
74HC/T374	OCT D-TYPE F/F POS EDGE TRIG, 3-S	20	A		A
74HC/T377	OCT D-TYPE F/F/ENABLE, POS EDG T	20	A		A
74HC/T390	DUAL DECADE RIPPLE COUNTER	16	A	A	A
74HC/T393	DUAL 4-BIT BINARY RIPPLE COUNTER	14	A		A
74HC4002	DUAL 4-INPUT NOR GATE	14	A	A	A
74HC/T40103	8-BIT SYNCH DON COUNTER	16	A		A
74HC/T40104	4 BIT BIDIRECT UNIV RGSTR	16	A		A
74HC/T40105	4 BIT X 16-ORD FIFO REGISTER	16	A		A
74HC4015	DUAL 4-BIT SHIFT REGISTER	16	A		A
74HC4016	QUAD BILATERAL SITCH	14	A	A	A
74HC4017	JOHNSON COUNTER/10 OUTPUTS	16	A	A	A
74HC/T4020	14-STAGE BINARY RIPPLE COUNTER	16	A		A
74HC/T4024	7-STAGE BINARY RIPPLE COUNTER	14	A	A	A
74HC/T4040	12-STAGE BINARY RIPPLE COUNTER	16	A		A
74HC4046A	PHASE LOCKED LOOP/VCO	16	A	A	A
74HC4049	HEX INV HIGH-LO LEVEL SHIFTER	16	A	A	A
74HC4050	HEX HIGH-LO LEVEL SHIFTER	16	A		A
74HC/T4051	8-CHANNEL ANALOG MUX/DEMUX	16	A	A	A
74HC/T4052	DUAL 4-CHANNEL ANALOG MUX/DMUX	16	A	A	A
74HC/T4053	TRIPLE 2-CHANNEL MUX/DEMUX	16	A	A	A
74HCT4059	PROGRAMMABLE DIVIDE-BY-N COUNTER	24	A		A
74HC/T4060	14-STAGE BINARY RIPPLE COUNTER	16	A	A	A
74HC/T4066	QUAD BILATERAL SITCH	14	A	A	A
74HC/T4067	16-CHANNEL ANALOG MUX/DEMUX	24	A		A
74HC/T4075	TRIPLE 3-INPUT OR GATE	14	A	A	A
74HC/T4094	8-STAGE SHIFT-&-STORE BUS REG	16	A		A
74HC/T42	BCD-TO-DECIMAL DECODER (1 OF 10)	16	A	A	A
74HC/T423	DUAL RETRIG MONOSTBL MULTIVIB	16	A		A
74HC/T4316	QUAD BILATERAL SITCH	16	A	A	A
74HC/T4351	8-CHANNEL ANALOG MUX/DEMUX	20	A	A	A
74HC4352	DUAL 4-CHAN MUX/DEMUX/LTCH	20	A		A
74HC4353	TRIPLE 2-CHAN MUX/DEMUX/LTCH	20	A	A	
74HC/T4510	BCD UP/DON COUNTER	16	A		A
74HC4511	BCD TO 7-SEG LATCH DECODR/DRVR	16	A	A	A
74HC4514	4-TO-16 LINE DECODER/MUX/LTCH	24	A	A	A
74HC4515	4-TO-16 LINE DECODER/DEMUX/LTCH	24	A		A
74HC/T4516	BINARY UP/DON COUNTER	16	A		A
74HC4518	DUAL BCD COUNTER	16	A		A
74HC/T4520	DUAL 4-BIT SYNCH BINARY COUNTER	16	A		A
74HC/T4538	DUAL RETRIG MONOSTBL MULTIVIB	16	A		A
74HC/T4543	BCD TO 7-SEG LATCH DECODR/DRVR	16	A		A
74HC533	OCTAL 3-STATE LATCH INVERTING	20	A		A
74HC/T534	OCT D-TYPE F/F INV, 3-STATE	20	A		A
74HC/T540	OCT BUFFER/LINE DRVR, INV 3-S	20	A		A
74HC/T541	OCT BUFFER/LINE DRVR, 3-S	20	A		A
74HC/T563	OCT D-TYPE TRANSP LATCH, INV 3-S	20	A	A	A
74HC/T564	OCT D-TYPE F/F POS EDGE TRIG, 3-S	20	A	A	A
74HC/T573	OCT D-TYPE TRANSPARENT LATCH	20	A		A
74HC/T574	OCT D-TYPE F/F POS EDGE TRIG, 3-S	20	A		A
74HC58	DUAL AND/OR GATE	14	A	A	
74HC583	BCD ADDER	16	A		A
74HC/T597	8-BIT SHIFT REG/INPUT LATCH	16	A	A	A
74HC/T640	OCTAL BUS TRANSCEIVER INV 3-S	20	A		A
74HC/T646	OCT BUS XCVR/REGISTER, 3-S	24	A	A	
74HC/T652	OCT BUS XCVR/REGISTER, 3-S	24	A		A
74HC670	4 X 4 REGISTER FILE, 3-STATE	16	A		A
74HC688	8-BIT MAGNITUDE COMPARATOR	20	A	A	A
74HC/T7030	64 WORD X 9-BIT FIFO	28	A		A
74HC/T7046A	PHASED-LOCKED LOOP/LOCK DTCT	16	A		A
74HC7266	QUAD 2-INPUT EXCLSVE-NOR GATE	14	A	A	A
74HC/T73	DUAL J-K MASTER SLAVE F/F	14	A	A	A
74HC/T74	DUAL D-TYPE EDGE TRIGGER F/F	14	A		A
74HC/T75	QUAD BISTABLE TRNSPT LATCH	16	A	A	A
74HC/T85	4-BIT MAGNITUDE COMPARATOR	16	A	A	A
74HC/T86	QUAD 2-INPUT EXCLUSIVE-OR GATE	14	A	A	A
74HC/T93	4-BIT BINARY RIPPLE COUNTER	14	A		A

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Philips Logic
Competitive Cross Reference Guide

HEF4000 Family

Features

- All parts available in DIP and SO
- Compatible with CD4000
- Committed to supply well into the next decades
- Low power, low speed
- Power supply 3 to 15V
- Easy to design
- Recent designs
  - HEF4794B 8-output LED driver
  - HEF4894B 12-output LED driver
  - HEF7069UB open drain inverter

HC/T Family

Features

- All parts available in HC and HCT (TTL input)
- 74HCTxxx replaces LS-TTL (74LSxxx)
- Low power, high speed
- Power supply 2.0 to 6.0V
- Analog switches 2.0 to 10V
  - 74HC4051, 4052, 4053
  - 74HC4351, 4352, 4353
  - 74HC4066, 4067, 4316
- Phase-Locked-Loop (PLL) experts
  - 74HC4046A, 7046A, 9046A
  - Free design software
  - Extensive application notes

AHC/T Family

Features

- 4 ns propagation delays
- 3x faster than HCMOS
- Operation down to 3.3V
- 16% less signal noise
- Consumes 75% less dynamic power and 50% less static power
- Full selection of functions are available
- All parts will be available in both SO and TSSOP

PicoGate Family

Features

- All parts available in HC/ HCT, AHC/AHCT
- Low power, high speed
- Power supply 2.0 to 6.0V
- Analog switches 2.0 to 10V
  - 74HC1G66/74HCT1G66
- Extended temperature range from -40 to 125° C
- LVC family release in 2000
- Great for ASIC repairs
- Perfect for when space is a concern
- 30% smaller than other single gate packages on the market

AVC Family

Features

- 1.0ns performance
- Optimized for 2.5V output
- -8/8mA static output drive
- High dynamic drive
- 20µA standby current
- V_{CC}: 1.2 – 3.3V
- 3.6 tolerant I/Os
- Live insertion
- Bus hold option

LVC Family

Features

- Low Voltage CMOS
- 74LVCxxx 3.3V equivalent of FAST
- High speed, medium drive
- 5V tolerant I/Os
- Direct interface with TTL levels
- Power supply 1.2 to 3.6V
- Live insertion
- Bus hold option
- Damping resistor option

ALVC Family

Features

- Fastest CMOS based family
- 2 ns propagation delays
- Power supply 1.2 to 3.6V
- -24/24mA drive capability
- 40µA standby current
- 5V tolerant
- Bus hold option
- Non-bus hold types are 5V tolerant
- Termination resistor option
- Bus Interface functions

Supports memory interfacing. Frequently used in high speed telecom applications.

LV Family

Features

- Largest low voltage family available
- 74LVxxx replaces 74HCxxx at V_{CC}= 3.3V
- Low power, high speed
- Low EMI (radiation)
- Power supply 1.0 to 5.5V
- Operates at V_{CC} = 5V
  - Speed 2 x HCMOS
  - Drive 2 X HCMOS
- Analog switches 1.0 to 6.0V
  - At V_{CC}= 5V R-ON 50% of HCMOS
  - 74LV4051, 4052, 4053
  - 74LV4066, 4067, 4316
- Battery charger NiMH and NiCd
  - V_{CC} = 0.9 to 6.0V
  - 1 to 4 batteries

ABT/ABT–16 5V Family

Features

- 3ns performance
- 32-64mA drive
- 250uA standby current
- Power supply 4.5V-5.5V
- Live insertion
- Bus hold option
- Termination resistor option

LVT/LVT–16 3V and ALVT 2.5/3/5V Families

Features

- Worlds fastest TTL Logic
- Ultra high speed 190-270MHz
- High Drive 64mA Output Drive
- Standard TTL functions and pin outs
- -45 to 85 deg C Operating Range
- Live insertion
- Bus hold option
- Termination resistor option
- Pin compatible with existing ABT & LVT
- Mixed I/O compatible from 2.5 to 5V

All Specifications available in Philips 1998 BiCMOS Bus Interface Manual (IC23) and on the Philips web site at www.philipslogic.com

ALS Family

Features

- 4ns propagation delays
- Guaranteed AC performance over temperature and extended V_{CC} range: 5V +/- 10%
- High Impedance PNP base input structure for reduced bus loading in low state
- Standard TTL functions and pin outs
- Replacement for LS types are 1/2 the power with twice the speed
- 2kV ESD protection

FAST Family

Features

- More than 238 functions available
- Standard TTL functions and pinouts
- High speed 3nSec. prop. Delay
- Power supply 5V+/- 10%

Special functions:
High Current Buffer/Transceiver
Light loaded input Structure
Immune Metastable Flip/Flop, Dram Controllers
Octal/Buffer, Transceiver with parity

FBL (Future Bus Low Voltage) Family

Features

- 3.3V BiCMOS bus transceiver
- High drive capability 100mA
- Same pin out, function & features as 5V FB
- Permits incident wave switching in heavily loaded back planes
- 70% less power usage vs. 5V FB
- Low noise

Used in EDP & telecom systems requiring high drive output and incident wave switching

Philips Logic
Competitive Cross Reference Guide

FAMILY	PACKAGE	PHILIPS	TI	FAIRCHILD	ON SEMI	TOSHIBA
CMOS						
4000	DIP SOIC SSOP I SSOP II TSSOP I	HEF4xxxBPN HEF4xxxBTD HEF4xxxDB 	CD4xxxBE CD4xxxBM 	CD4xxxBN CD4xxxBM/WM CD4xxxMTC	MC14xxxBP MC14xxxBD MC14xxxDT	TC4xxxBP TC4xxxBFN TC4xxxFS
HC(T) T=TTL FUNCTION	DIP SOIC SSOP II TSSOP I	74HC(T)xxxN 74HC(T)xxxD 74HC(T)xxxDB 74HC(T)xxxPW	SN74HC(T)xxxN SN74HC(T)xxxD/DW SN74HC(T)xxxDB SN74HC(T)xxxPW	MM74HC(T)xxxN MM74HC(T)xxxM/WM MM74HC(T)xxxMTC	MC74HC(T)xxxN MC74HC(T)xxxD MC74HC(T)xxxDT	TC74HC(T)xxxAP TC74HC(T)xxxAFW
AHC(T)	SOIC TSSOP I	74AHC(T)xxxD 74AHC(T)xxxPW	SN74AHC(T)xxxD/DW SN74AHC(T)xxxPW	MM74VHC(T)xxxM/WM MM74VHC(T)xxxMTC	MC74VHC(T)xxxD MC74VHC(T)xxxDT	TC74VHC(T)xxxAFN/FW TC74VHC(T)xxxAFT
PICOGATE (Single Gate Logic)						
HC Series	SOT353-5	74HC1GxxxGW		NC7SxxxM5		TC7SxxxFU
HCT Series	SOT353-5	74HCT1GxxxGW		NC7STxxxM5		TC7STxxxFU
AHC Series	SOT353-5	74AHC1GxxxGW	SN74AHC1GxxxDCK		MC74VHC1GxxxDFT1	TC7SHxxxFU
AHCT Series	SOT353-5	74AHCT1GxxxGW	SN74AHCT1GxxxDCK		MC74VHCT1GxxxDFT1	TC7SETxxxFU
LVC Series	SOT353-5	74LVC1GxxxGW	SN74LVC1GxxxDCK	NC7SZxxxM5		TC7SZxxxFU
Low Voltage CMOS						
LVC(H) H=bushold feature	SOIC SSOP II TSSOP I 48/56 PIN SSOP III 48/56 PIN TSSOP II LFGBA	74LVC(H)xxxAD 74LVC(H)xxxADB 74LVC(H)xxxAPW 74LVC(H)16xxxADL 74LVC(H)16xxxADGG 74LVC(H)32xxxAEC	SN74LVC(H)xxxAD/DW SN74LVC(H)xxxADB SN74LVC(H)xxxAPW SN74LVC(H)16xxxADL SN74LVC(H)16xxxADGG SN74LVC(H)32xxxAGKE	74LCXxxxM/WM 74LCXxxxMSA 74LCXxxxMTC 74LCX16xxxMEA 74LCX16xxxMTD	MC74LCXxxxD MC74LCXxxxSD MC74LCXxxxDT MC74LCX16xxxDT	TC74LCXxxxFN/FW TC74LCXxxxFT TC74LCX16xxxFT
ALVC(H)	48/56 PIN SSOP III 48/56 PIN TSSOP II LFBGA	74ALVC(H)16xxxDL 74ALVC(H)16xxxDGG 74ALVC(H)32xxxEC	SN74ALVC(H)16xxxDL SN74ALVC(H)16xxxDGG SN74ALVC(H)32xxxGKE	74VCX16xxxMEA 74VCX16xxxMTD		TC74LCX16xxxFT
LV	SOIC SSOP II TSSOP I	74LVxxxD 74LVxxxDB 74LVxxxPW	SN74LVxxxD/DW SN74LVxxxDB SN74LVxxxPW	74LVXxxxM/WM 74LVXxxxMSA 74LVXxxxMTC	MC74LVXxxxD MC74LVXxxxDT	TC74LVXxxxFN/FW TC74LVXxxxFS TC74LVXxxxFT
AVC	TSSOP LFBFA	74AVC16xxxDGG 74AVC32xxxEC	SN74AVC16xxxDGG SN74AVC32xxxGKE			
BiCMOS						
ABT(H) H=bushold feature	DIP SOIC SSOP II TSSOP I 48/56 PIN SSOP III 48/56 PIN TSSOP II	74ABTxxxN 74ABTxxxD 74ABTxxxDB 74ABTxxxPW 74ABT(H)16xxxDL 74ABT(H)16xxxDGG	SN74ABTxxxN SN74ABTxxxD/DW SN74ABTxxxDB SN74ABTxxxPW SN74ABT(H)16xxxDL SN74ABT(H)16xxxDGG	74ABTxxxPC 74ABTxxxSC 74ABTxxxMSA 74ABTxxxMTC 74ABT16xxxSSC 74ABT16xxxMTD		
Low Voltage BiCMOS						
LVT Bushold is built in	SOIC SSOP II TSSOP I 48/56 PIN SSOP III 48/56 PIN TSSOP II	74LVTxxxD 74LVTxxxDB 74LVTxxxPW 74LVT16xxxDL 74LVT16xxxDGG	SN74LVTxxxD/DW SN74LVTxxxDB SN74LVTxxxPW SN74LVT16xxxDL SN74LVT16xxxDGG	74LVTxxxM/WM 74LVTxxxMSA 74LVTxxxMTC 74LVT16xxxMEA 74LVT16xxxMTD		
ALVT Bushold is built in	48/56 PIN SSOP III 48/56 PIN TSSOP II	74ALVT16xxxDL 74ALVT16xxxDGG	SN74ALVT16xxxDL SN74ALVT16xxxDGG			
BIPOLAR						
ALS	DIP SOIC SSOP II	74ALSxxxN 74ALSxxxD 74ALSxxxDB	SN74ALSxxxN SN74ALSxxxD/DW SN74ALSxxxDB	DM74ALSxxxN DM74ALSxxxM/WM DM74ALSxxxMSA		
FAST	DIP SOIC SSOP II	N74FxxxN N74FxxxD N74FxxxDB	SN74FxxxN SN74FxxxD/DW SN74FxxxDB	74FxxxPC/SPC 74FxxxSC 74FxxxMSA		
SPECIALTY LOGIC						
FBL (3.3V BTL)	52 PIN PQFP	FBLxxxxBB				

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