MOSFET

General form

```
M<name> <drain node> <gate node> <source node>
+ <bulk/substrate node> <model name>
+ [L=<value>] [W=<value>]
+ [AD=<value>] [AS=<value>]
+ [PD=<value>] [PS=<value>]
+ [NRD=<value>] [NRS=<value>]
+ [NRG=<value>] [NRB=<value>]
+ [M=<value>] [N=<value>]
```

Examples

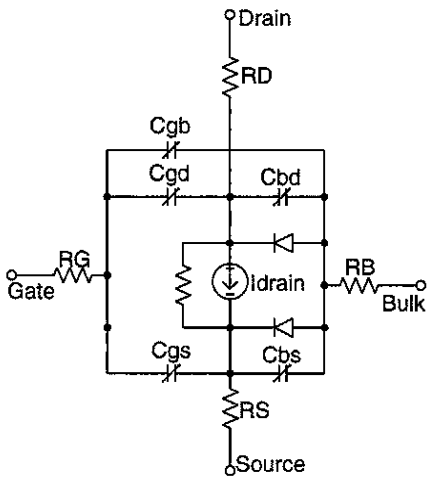
```
M1 14 2 13 0 PNOM  L=25u W=12u
M13 15 3 0 0 PSTRONG
M16 17 3 0 0 PSTRONG M=2
M28 0 2 100 100 NWEAK L=33u W=12u
+ AD=288p AS=288p PD=60u PS=60u NRD=14 NRS=24 NRG=10
```

Model form

```
.MODEL <model name> NMOS [model parameters]
.MODEL <model name> PMOS [model parameters]
```

Description

The MOSFET is modeled as an intrinsic MOSFET using ohmic resistances in series with the drain, source, gate, and bulk (substrate). There is also a shunt resistance (RDS) in parallel with the drain-source channel.



Arguments and options

L and W

are the channel length and width, which are decreased to get the effective channel length and width. They can be specified in the device, **.MODEL (model definition)**, or **.OPTIONS (analysis options)** statements. The value in the device statement supersedes the value in the model statement, which supersedes the value in the .OPTIONS statement. Defaults for L and W can be set in the .OPTIONS statement. If L or W defaults are not set, their default value is 100 u.

[L=<value>] [W=<value>] cannot be used in conjunction with Monte Carlo analysis.

Chapter

AD and AS
The drain and source diffusion areas. Defaults for AD and AS can be set in the .OPTIONS statement. If AD or AS defaults are not set, their default value is 0.

PD and PS
The drain and source diffusion perimeters. Their default value is 0.

JS
Can specify the drain-bulk and source-bulk saturation currents. JS is multiplied by AD and AS.

IS
Can also specify the drain-bulk and source-bulk saturation currents. IS is an absolute value.

CJ
Can specify the zero-bias depletion capacitances. CJ is multiplied by AD and AS.

CJSW
Can also specify the zero-bias depletion capacitances. CJSW is multiplied by PD and PS.

CBD and CBS
Can also specify the zero-bias depletion capacitances. CBD and CBS are absolute values.

NRD, NRS, NRG, and NRB
Multipliers (in units of squares) that can be multiplied by RSH to yield the parasitic (ohmic) resistances of the drain (RD), source (RS), gate (RG), and substrate (RB), respectively. NRD, NRS, NRG, and NRB default to 0.

Consider a square sheet of resistive material. Analysis shows that the resistance between two parallel edges of such a sheet depends upon its composition and thickness, but is *independent* of its size as long as it is *square*. In other words, the resistance will be the same whether the square's edge is 2 mm, 2 cm, or 2 m. For this reason, the sheet resistance of such a layer, abbreviated **RSH**, has units of ohms per square.

M (NP)
A parallel device multiplier (default = 1), which simulates the effect of multiple devices in parallel. (NP is an alias for M.)

The effective width, overlap and junction capacitances, and junction currents of the MOSFET are multiplied by M. The parasitic resistance values (e.g., RD and RS) are divided by M. Note the third example: it shows a device twice the size of the second example.

N (NS)

A series device multiplier (default value= 1.0) for the Level 5 model only, which simulates an approximation of the effect of multiple devices in series. NS is an aliased name for N.

There are some things to keep in mind while using this parameter. The parameter N is used to derive the effective length, Leff = N · (L+DL), of a transistor drawn as N elements of width W and length L in series (in other words, the drain of element [K] is the source of element [K+1], and the gates are tied together). The short-channel effects included in the pinch-off voltage calculation, however, are evaluated using the effective length L+DL of each element. Except for this, everything is calculated as if the transistor were laid out as a single element of length L=Leff-DL=N · (L+DL)-DL.

In this compact formulation, the intermediate drain/source diffusions appearing along the channel are ignored (that is, junction capacitance and diffusion resistances are assumed to be zero). As a consequence, DC, AC and transient analyses can yield different results compared with the standard device declaration, particularly at higher frequencies. A closer match is obtained for long devices, or devices with low RS and RD and high UCRIT. Be sure to evaluate the accuracy of this compact formulation and to check the validity of the underlying approximations.

Comments

The simulator provides six MOSFET device models, which differ in the formulation of the I-V characteristic. The **LEVEL** parameter selects among different models as shown below. For more information, see **References**.

- **LEVEL**=1 Shichman-Hodges model (see reference [1])
- **LEVEL**=2 geometry-based, analytic model (see reference [2])
- **LEVEL**=3 semi-empirical, short-channel model (see reference [2])
- **LEVEL**=4 BSIM model (see reference [3])
- **LEVEL**=5 EKV model version 2.6 (see reference [10])
- **LEVEL**=6 BSIM3 model version 2.0 (see reference [7])
- **LEVEL**=7 BSIM3 model version 3.1 (see reference [8])

Capture parts

The following table lists the set of MOSFET breakout parts designed for customizing model parameters for simulation. These are useful for setting up Monte Carlo and worst-case analyses with device and/or lot tolerances specified for individual model parameters.

Part name	Model type	Property	Property description
MBREAKN	NMOS	L	channel length
MBREAKN3		W	channel width
MBREAKN4		AD	drain diffusion area
MBREAKP	PMOS	AS	source diffusion area
MBREAKP3		PD	drain diffusion perimeter
MBREAKP4		PS	source diffusion perimeter
		NRD	relative drain resistivity (in squares)
		NRS	relative source resistivity (in squares)
		NRG	relative gate resistivity (in squares)
		NRB	relative substrate resistivity (in squares)
		M	device multiplier (simulating parallel devices)
		MODEL	NMOS or PMOS model name

Setting operating temperature

Operating temperature can be set to be different from the global circuit temperature by defining one of the model parameters: T_ABS, T_REL_GLOBAL, or T_REL_LOCAL. Additionally, model parameters can be assigned unique measurement temperatures using the T_MEASURED model parameter. For more information, see **MOSFET model parameters**.

MOSFET model parameters

For all model levels

The parameters common to all model levels are primarily parasitic element values such as series resistance, overlap and junction capacitance, and so on.

Model levels 1, 2, and 3

The DC characteristics of the first three model levels are defined by the parameters **VTO**, **KP**, **LAMBDA**, **PHI**, and **GAMMA**. These are computed by the simulator if process parameters (e.g., **TOX**, and **NSUB**) are given, but the user-specified values always override. **VTO** is positive (negative) for enhancement mode and negative (positive) for depletion mode of N-channel (P-channel) devices.

The default value for **TOX** is 0.1 μ for Levels 2 and 3, but is unspecified for Level 1, which discontinues the use of process parameters.

For MOSFETs the capacitance model has been changed to conserve charge, affecting only the Level 1, 2, and 3 models.

Effective length and width for device parameters are calculated with the formula:

$P_i = P_0 + P_L/L_e + P_W/W_e$

where:

L_e = effective length = L - (LD · 2)
W_e = effective width = W - (WD · 2)

See .MODEL (model definition) for more information.

Model level 4

Unlike the other models in PSpice, the BSIM model is designed for use with a process characterization system that provides all parameters. Therefore, there are no defaults specified for the parameters, and leaving one out can cause problems.

The **LEVEL**=4 (BSIM1) model parameters are all values obtained from process characterization, and can be generated automatically. Reference [4] of References describes a means of generating a process file, which must then be converted into .MODEL (model definition) statements for inclusion in the Model Library or circuit file. (The simulator does not read process files.)

The level 4 (BSIM) and level 6 (BSIM3 version 2) models have their own capacitance model, which conserves charge and remains unchanged. References [6] and [7] describe the equations for the capacitance due to channel charge.

In the following MOSFET model parameters list, parameters marked with a ζ in the Default column also have corresponding parameters with a length and width dependency. For

example, VFB is a basic parameter using units of volts, and LVFB and WVFB also exist and have units of volt·μ. The formula

$P_i = P_0 + P_L/L_e + P_W/W_e$

is used to evaluate the parameter for the actual device, where:

L_e = effective length = L - DL
W_e = effective width = W - DW

Model level 5 (EKV version 2.6)

The EKV model is a scaleable and compact model built on fundamental physical properties of the device. Use this model to design low-voltage, low-current analog, and mixed analog-digital circuits that use sub-micron technologies. The charge-based static, quasi-static dynamic, and noise models are all derived from the normalized transconductance-to-current ratio, which is accurately described for all levels of current, including the moderate inversion region. A single I-V expression preserves the continuity of first- and higher-order derivatives with respect to any terminal voltage in all regions of device operation.

Version 2.6 models the following:

- geometrical and process related aspects of the device (oxide thickness, junction depth, effective channel length and width, and so on)
- effects of doping profile and substrate effects
- weak, moderate, and strong inversion behavior
- mobility effects due to vertical and lateral fields and carrier velocity saturation
- short-channel effects such as channel-length modulation, source and drain charge sharing, and the reverse short channel effect
- thermal and flicker noise modeling
- short-distance geometry and bias-dependent device matching for Monte Carlo analysis.

For more detailed model information, see reference [10] of References.

Additional notes

Note 1

The **DL** and **DW** parameters usually have a negative value.

Note 2

0 (zero) and O (the letter O) are not interchangeable. For example, use **VTO**, not **VT0** (**VTO** is referenced to the bulk); use **E0**, not **EO**; use **Q0**, not **QO**.

Note 3

Use the **AVTO**, **AKP**, and **AGAMMA** model parameters with a DEV tolerance to perform Monte Carlo and Sensitivity/Worst-Case analyses. Their default values cannot be changed.

The device-to-device matching of MOSFETs depends on the gate area, W · L. Using **AVTO**, **AKP**, and **AGAMMA** with a DEV tolerance applies the matching scaling law for the model equations and derives the device matching statistics (DEV tolerance) from a single normalized parameter. (Without these parameters, you would need to use a dedicated .MODEL card with a DEV tolerance for **VTO**, **KP** and **GAMMA** for each value of the gate area used in your design.)

Do not apply the LOT specification, which is a measure of the ability of the process to control the absolute value of a model parameter, to **AVTO**, **AKP**, and **AGAMMA**, because this would be redundant with the LOT specification for **VTO**, **KP**, and **GAMMA**.

Note 4 Use the model parameter **HDIF** with the device parallel multiplier, M, to set default values for **AD**, **AS**, **PD**, and **PS**. Use **HDIF** only for the MOSEKV (Level 5) model.

When **HDIF** is specified, the following equations are used.

$$\mathbf{NRD} = \mathbf{HDIF}/W$$

$$\mathbf{NRS} = \mathbf{HDIF}/W$$

For M = 1, the following equations are used.

$$\mathbf{AD} = (2 \cdot \mathbf{HDIF}) \cdot W$$

$$\mathbf{AS} = (2 \cdot \mathbf{HDIF}) \cdot W$$

$$\mathbf{PD} = 2 \cdot ((2 \cdot \mathbf{HDIF}) + W)$$

$$\mathbf{PS} = 2 \cdot (2 \cdot \mathbf{HDIF}) + W$$

For M ≥ 2 and even:

$$\mathbf{AD} = \mathbf{HDIF} \cdot W$$

$$\mathbf{AS} = (\mathbf{HDIF} + (2 \cdot \mathbf{HDIF})/M) \cdot W$$

$$\mathbf{PD} = (2 \cdot \mathbf{HDIF}) + W$$

$$\mathbf{PS} = (2 \cdot \mathbf{HDIF}) + W + 2 \cdot ((2 \cdot \mathbf{HDIF}) + W)/M$$

For M ≥ 2 and odd:

$$\mathbf{AD} = (\mathbf{HDIF} + (\mathbf{HDIF}/M)) \cdot W$$

$$\mathbf{AS} = (\mathbf{HDIF} + (\mathbf{HDIF}/M)) \cdot W$$

$$\mathbf{PD} = (2 \cdot \mathbf{HDIF}) + W + ((2 \cdot \mathbf{HDIF}) + W)/M$$

$$\mathbf{PS} = (2 \cdot \mathbf{HDIF}) + W + ((2 \cdot \mathbf{HDIF}) + W)/M$$

Note 5 If RGSH is specified, the default value for NRG is set to 0.5 · W/L.

Note 6 The model parameters **TOX**, **NSUB**, **VFB**, **UO**, and **VMAX** accomodate scaling behavior of the process and basic intrinsic model parameters, as well as statistical circuit simulation. These parameters are only used if **COX**, **GAMMA**, and/or **PHI**, **VTO**, **KP**, and **UCRIT** are not specified, respectively. Furthermore, a simpler mobility reduction model due to vertical field is accessible through the mobility reduction coefficient, **THETA**. **THETA** is only used if **E0** is not specified.

Model level 6 (BSIM3 version 2.0)

The Level 6 Advanced parameters should not be changed unless the detail structure of the device is known and has specific, meaningful values.

The BSIM3 model is a physical model using extensive built-in dependencies of important dimensional and processing parameters. It includes the major effects that are important to modeling deep-submicrometer MOSFETs, such as threshold voltage reduction, nonuniform doping, mobility reduction due to the vertical field, bulk charge effect, carrier velocity saturation, drain-induced barrier lowering (DIBL), channel length modulation (CLM), hot-carrier-induced output resistance reduction, subthreshold conduction, source/drain parasitic resistance, substrate current induced body effect (SCBE), and drain voltage reduction in LDD structure. For additional, detailed model information, see **References**.

Additional notes

Note 1 If any of the following BSIM3 version 2.0 model parameters are not explicitly specified, they are calculated using the following equations.

$$\mathbf{VTH0} = \mathbf{VFB} + \mathbf{PHI} + \mathbf{K}\sqrt{\mathbf{PHI}}$$

$$\mathbf{K1} = \mathbf{GAMMA2} - 2 \cdot \mathbf{K2}\sqrt{(\mathbf{PHI} - \mathbf{VBM})}$$

$$\mathbf{K2} = \frac{(\mathbf{GAMMA1} - \mathbf{GAMMA2})(\sqrt{\mathbf{PHI} - \mathbf{VBX}} - \sqrt{\mathbf{PHI}})}{2\sqrt{\mathbf{PHI}}(\sqrt{\mathbf{PHI} - \mathbf{VBX}} - \sqrt{\mathbf{PHI}}) + \mathbf{VBM}}$$

$$\mathbf{VBF} = \mathbf{VTH0} - \mathbf{PHI} - \mathbf{K1}\sqrt{\mathbf{PHI}}$$

$$\mathbf{PHI} = 2V_{tm}\ln\left(\frac{\mathbf{NPEAK}}{n_i}\right)$$

$$\mathbf{GAMMA1} = \frac{\sqrt{2q\varepsilon_{si}\mathbf{NPEAK}}}{\mathbf{COX}}$$

$$\mathbf{GAMMA2} = \frac{\sqrt{2q\varepsilon_{si}\mathbf{NSUB}}}{\mathbf{COX}}$$

$$\mathbf{VBX} = \mathbf{PHI} - q \cdot \mathbf{NPEAK} \cdot \mathbf{XT}^2/(2\varepsilon_{si})$$

$$\mathbf{LITL} = \sqrt{\frac{\varepsilon_{si}\mathbf{TOXX}_j}{\varepsilon_{ox}}}$$

Note 2 Default values listed for the BSIM3 version 2.0 parameters **UA**, **UB**, **UC**, **UA1**, **AB1**, and **UC1** are used for simplified mobility modeling.

Model level 7 (BSIM3 version 3.1)

The BSIM3 version 3.1 model was developed by the University of California, Berkeley, as a deep submicron MOSFET model with the same physical basis as the BSIM3 version 2 model, but with a number of major enhancements, such as a single I-V expression to describe current and output conductance in all regions of device operation, better modeling of narrow width devices, a reformulated capacitance model to improve short and narrow geometry models, a

new relaxation time model to improve transient modeling, and improved model fitting of various W/L ratios using one parameter set. BSIM3 version 3.1 retains the extensive built-in dependencies of dimensional and processing parameters of BSIM3 version 2. For additional, detailed model information, see Reference [8] of **References**.

Additional notes

Note 1

If any of the following BSIM3 version 3.1 model parameters are not explicitly specified, they are calculated using the following equations:

If **VTHO** is not specified, then:

$$\mathbf{VTHO} = \mathbf{VFB} + \phi_s \mathbf{K1}\sqrt{\phi_s}$$

where:

VFB=-1.0

If **VTHO** is specified, then:

$$\mathbf{VFB} = \mathbf{VTHO} - \phi_s + \mathbf{K1}\sqrt{\phi_s}$$

$$\mathbf{VBX} = \phi_s - \frac{q \cdot \mathbf{NCH} \cdot XT^2}{2 \cdot \varepsilon_{si}}$$

$$\mathbf{CF} = \left(\frac{2\varepsilon_{ox}}{\pi}\right)\ln\left(1 + \frac{4 \times 10^{-7}}{\mathbf{TOX}}\right)$$

where

$E_g(T)$=the energy bandgap at temperature T= $1.16 - \frac{(7.02 \cdot 10^{-4} \cdot T^2)}{(T + 1108)}$

Note 2

If **K1** AND **K2** are not specified, they are calculated using the following equations:

$$\mathbf{K1} = \mathbf{GAMMA2} - 2\mathbf{K2}\sqrt{\phi_s - \mathbf{VBM}}$$

$$\mathbf{K2} = \frac{(\mathbf{GAMMA1} - \mathbf{GAMMA2})(\sqrt{\phi_S - \mathbf{VBX}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - \mathbf{VBM}} - \sqrt{\phi_s}) + \mathbf{VBM}}$$

where:

$$\phi_s = 2Vt \cdot \ln\left(\frac{\mathbf{NCH}}{n_i}\right)$$

$$Vt = \frac{k \cdot T}{q}$$

$$n_i = 1.45 \cdot 10^{10}\left(\frac{T}{300.15}\right)^{1.5} \qquad \exp\left(21.5565981 - \frac{E_g(T)}{2Vt}\right)$$

Note 3

If **NCH** is not given and **GAMMA1** is given, then:

$$\mathbf{NCH} = \frac{\mathbf{GAMMA1}^2 \cdot (Cox)^2}{2q \cdot \varepsilon_{si}}$$

If neither **GAMMA1** nor **NCH** is given, then **NCH** has a default value of 1.7e23 $1/m^3$ and **GAMMA1** is calculated from **NCH**:

$$\mathbf{GAMMA1} = \frac{\sqrt{2q \cdot \varepsilon_{si} \cdot \mathbf{NCH}}}{Cox}$$

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
T_ABS †	absolute temperature	°C	
T_MEASURED †	measured temperature	°C	
T_REL_GLOBAL †	relative to current temperature	°C	
T_REL_LOCAL †	relative to AKO model temperature	°C	
W	channel width	meter	**DEFW**
	levels 1, 2, and 3		
DELTA	width effect on threshold		0
ETA	static feedback (Level 3)		0
GAMMA	bulk threshold parameter	$volt^{1/2}$	see page 178
KP	transconductance coefficient	$amp/volt^2$	2.0E-5
KAPPA	saturation field factor (Level 3)		0.2
LAMBDA	channel-length modulation (Levels 1 and 2)	$volt^{-1}$	0.0
LD	lateral diffusion (length)	meter	0.0
NEFF	channel charge coefficient (Level 2)		1.0
NFS	fast surface state density	$1/cm^2$	0.0
NSS	surface state density	$1/cm^2$	none
NSUB	substrate doping density	$1/cm^3$	none
PHI	surface potential	volt	0.6
THETA	mobility modulation (Level 3)	$volt^{-1}$	0.0
TOX	oxide thickness	meter	see page 178
TPG	Gate material type: +1 = opposite of substrate -1 = same as substrate 0 = aluminum		+1
UCRIT	mobility degradation critical field (Level 2)	volt/cm	1.0E4
UEXP	mobility degradation exponent (Level 2)		0.0
UTRA	(not used) mobility degradation transverse field coefficient		0.0
UO	surface mobility (The second character is the letter O, not the numeral zero.)	$cm^2/volt{\cdot}sec$	600
VMAX	maximum drift velocity	meter/sec	0

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
X2U1	Sens. of velocity saturation effect to substrate bias	μ/volt^2	ζ
X3E	Sens. of drain-induced barrier lowering effect to drain bias @ Vds = Vdd	volt^{-1}	ζ
X3MS	Sens. of mobility to drain bias @ Vds=Vdd	cm^2/volt^2·sec	ζ
X3U1	Sens. of velocity saturation effect on drain	μ/volt^2	ζ
XPART	Gate-oxide capacitance charge model flag. **XPART**=0 selects a 40/60 drain/source charge partition in saturation, while **XPART**=1 selects a 0/100 drain/source charge partition.		
	level 5: process parameters		
COX	gate oxide capacitance per unit area	F/m^2	0.7E-3
XJ	junction depth	m	0.1E-6
DW	channel width correction	m	0.0 see page 179
DL	channel length correction	m	0.0 see page 179
HDIF	length of heavily doped diffusion contact to gate	m	0.0 see page 179
	level 5: basic intrinsic parameters		
VTO	long-channel threshold voltage	V	0.5 see page 179
GAMMA	body effect parameter	$\sqrt{V}$	1.0
PHI	bulk Fermi potential (·2)	V	0.7
KP	transconductance parameter	A/V^2	50.0E-6
E0	mobility reduction coefficient	V/m	1.0E12 see page 179
UCRIT	longitudinal critical field	V/m	2.0E6
	level 5: channel length modulation and charge sharing parameters		
LAMBDA	depletion length coefficient (channel length modulation)		0.5
WETA	narrow-channel effect coefficient		0.25
LETA	short-channel effect coefficient		0.1

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
	level 5: impact ionization related parameters		
IBA	first impact ionization coefficient	1/m	0.0
IBB	second impact ionization coefficient	V/m	3.0E8
IBN	saturation voltage factor for impact ionization		1.0
	level 5: intrinsic temperature parameters		
TCV	threshold voltage temperature coefficient	V/K	1.0E-3
BEX	mobility temperature exponent		-1.5
UCEX	longitudinal critical field temperature exponent		0.8
IBBT	temperature coefficient for IBB	1/K	9.0E-4
	level 5: matching parameters		
AVTO	area related threshold voltage temperature coefficient	V·m	1.0E-6 see page 179
AKP	area related gain mismatch parameter	m	1.0E-6 see page 179
AGAMMA	area related body effect mismatch parameter	$\sqrt{V} \cdot m$	1.0E-6 see page 179
	level 5: resistance parameters		
RBC	bulk contact resistance	ohm	0.0
RBSH	bulk layer sheet resistance	ohm/square	0.0
RDC	drain contact resistance	ohm	0.0
RGC	gate contact resistance	ohm	0.0
RGSH	gate layer sheet resistance	ohm/square	0.0 see page 180
RSC	source contact resistance	ohm	0.0
	level 5: temperature parameters		
TR1	first-order temperature coefficient for drain, source series resistance	$°C^{-1}$	0.0
TR2	second-order temperature coefficient for drain, source series resistance	$°C^{-2}$	0.0
TRB	temperature coefficient for bulk series resistance	$°C^{-1}$	0.0
TRG	temperature coefficient for gate series resistance	$°C^{-1}$	0.0
XTI	drain, source junction current temperature exponent		0.0

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
	level 5: optional parameters		
NSUB	channel doping	meter	see page 180
THETA	mobility reduction coefficient	$volt^{-1}$	see page 180
TOX	oxide thickness	meter	see page 180
UO	low-field mobility	$\frac{cm^2}{volt \cdot sec}$	see page 180
VFB	flat-band voltage	volt	see page 180
VMAX	saturation velocity	meter/sec	see page 180
	level 5: setup parameters		
SATLIM	ratio defining the saturation limit i_f / i_r		54.6
	level 6		
A0	bulk charge effect coefficient NMOS		1.0
	bulk charge effect coefficient PMOS		4.4
A1	first non-saturation coefficient NMOS	1/V	0.0
	first non-saturation coefficient PMOS	1/V	0.23
A2	second non-saturation coefficient NMOS		1.0
	second non-saturation coefficient PMOS		0.08
AT	saturation velocity temperature coefficient	m/sec	3.3E4
BULKMOD	bulk charge model selector:		
	NMOS		1
	PMOS		2
CDSC	drain/source and channel coupling capacitance	F/m^2	2.4E-4
CDSCB	body bias sensitivity of CDSC	F/Vm^2	0.0
DL	channel length reduction on one side	m	0.0
DROUT	channel length dependent coefficient of the DIBL effect on Rout		0.56
DSUB	subthreshold DIBL coefficient exponent		DROUT
DVT0	first coefficient of short-channel effect on threshold voltage		2.2
DVT1	second coefficient of short-channel effect on threshold voltage		0.53
DVT2	body bias coefficient of short-channel effect on threshold voltage	1/V	-0.032

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
DW	channel width reduction on one side	m	0.0
ETA0	DIBL coefficient in subthreshold region		0.08
ETAB	body bias coefficient for the subthreshold DIBL coefficient	1/V	-0.07
K1	first-order body effect coefficient	$\sqrt{V}$	see page 181
K2	second-order body effect coefficient		see page 181
K3	narrow width effect coefficient		80.0
K3B	body effect coefficient of K3	1/V	0.0
KETA	body bias coefficient of the bulk charge effect.	1/V	-0.047
KT1	temperature coefficient for threshold voltage	V	-0.11
KT1L	channel length sensitivity of temperature coefficient for threshold voltage.	V-m	0.0
KT2	body bias coefficient of the threshold voltage temperature effect		0.022
NFACTOR	subthreshold swing coefficient		1.0
NGATE	poly gate doping concentration	$1/cm^3$	
NLX	lateral nonuniform doping coefficient	m	1.74E-7
NPEAK	peak doping concentration near interface	$1/cm^3$	1.7E17
NSUB	substrate doping concentration	$1/cm^3$	6.0E16
PCLM	channel length modulation coefficient		1.3
PDIBL1	first output resistance DIBL effect coefficient		0.39
PDIBL2	second output resistance DIBL effect coefficient		0.0086
PSCBE1	first substrate current body effect coefficient	V/m	4.24E8
PSCBE2	second substrate current body effect coefficient	m/V	1.0E-5
PVAG	gate dependence of Early voltage		0.0
RDS0	contact resistance	ohms	0.0
RDSW	parasitic resistance per unit width	ohms/ μ m	0.0
SATMOD	saturation model selector: For semi-empirical output: resistance model 1 For physical output: resistance model 2		2

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
SUBTHMOD	subthreshold model selector: no subthreshold model 0 BSIM1 subthreshold model 1 BSIM3 subthreshold model 2 BSIM3 subthreshold model using log current 3		2
TNOM	temperature at which parameters are extracted.	deg. C	27
TOX	gate oxide thickness	m	1.5E-8
UA	first-order mobility degradation coefficient	m/V	2.25E-9
UA1	temperature coefficient for **UA**	m/V	4.31E-9
UB	second-order mobility degradation coefficient	$(m/V)^2$	5.87E-19
UB1	temperature coefficient for **UB**	$(m/V)^2$	-7.61E-18
UC	body effect mobility degradation coefficient	1/V	0.0465
UC1	temperature coefficient for **UC**	1/V	-0.056
UTE	mobility temperature exponent		-1.5
VOFF	offset voltage in subthreshold region	V	-0.11
VSAT	saturation velocity at Temp=**TNOM**	cm/sec	8.0E6
VTH0	threshold voltage at Vbs=0 for large channel length	V	see page 181
W0	narrow width effect parameter	m	2.5E-6
XJ	junction depth	m	1.5E-7
XPART	charge partitioning coefficient: no charge model < 0.0 40/60 partition = 0.0 50/50 partition = 0.5 0/100 partition = 1.0		0.0
	level 6 advanced		
CIT	capacitance due to interface trapped charge	F/m^2	0.0
EM	critical electrical field in channel	V/m	4.1E7
ETA	drain voltage reduction coefficient due to LDD		0.3
GAMMA1	body effect coefficient near the interface	$\sqrt{V}$	see page 181
GAMMA2	body effect coefficient in the bulk	$\sqrt{V}$	see page 181
LDD	total length of the LDD region	m	0.0
LITL	characteristic length related to current depth	m	see page 181

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
PHI	surface potential under strong inversion	V	see page 181
U0	mobility at Temp=TNOM:		
	NMOS	cm^2/V-sec	670.0
	PMOS	cm^2/V-sec	250.0
VBM	maximum applied body bias	V	-5.0
VBX	vbs at which the depletion width equals XT	V	see page 181
VFB	flat-band voltage	V	see page 181
VGHIGH	voltage shift of the higher bound of the transition region	V	0.12
VGLOW	voltage shift of the lower bound of the transition region	V	-0.12
XT	doping depth	m	1.55E-7
level 7: control parameters			
CAPMOD	flag for the short-channel capacitance model	none	2
MOBMOD	mobility model selector	none	1
NOIMOD	flag for noise model	none	1
NQSMOD	flag for NQS model	none	0
PARAMCHK	flag for model parameter checking	none	0
level 7: AC and capacitance parameters			
CF	fringing field capacitance	F/m	see page 182
CKAPPA	coefficient for lightly doped region overlap capacitance fringing field capacitance	F/m	0.6
CLC	constant term for the short-channel model	m	0.1E-6
CLE	exponential term for the short-channel model	none	0.6
CGBO	gate-bulk overlap capacitance per unit channel length	F/m	0.0
CGDL	light-doped drain-gate region overlap capacitance	F/m	0.0
CGDO	non-LDD region drain-gate overlap capacitance per channel length	F/m	see page 183
CGSL	light-doped source-gate region overlap capacitance	F/m	0.0
CGSO	non-LDD region source-gate overlap capacitance per channel length	F/m	see page 183
CJ	bottom junction capacitance per unit area	F/m^2	5.0E-4

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
CJSW	source/drain side junction capacitance per unit periphery	F/m	5.0E-10
CJSWG	source/drain gate sidewall junction capacitance per unit width	F/m	CJSW
DLC	length offset fitting parameter from C-V	m	LINT
DWC	width offset fitting parameter from C-V	m	WINT
MJ	bottom junction capacitance grading coefficient	none	0.5
MJSW	source/drain side junction capacitance grading coefficient	none	0.33
MJSWG	source/drain gate sidewall junction capacitance grading coefficient	none	MJSW
PB	bottom built-in potential	V	1.0
PBSW	source/drain side junction built-in potential	V	1.0
PBSWG	source/drain gate sidewall junction built-in potential	V	PBSW
VFBCV	flat-band voltage parameter (for CAPMOD = 0 only)	V	-1.0
XPART	charge partitioning rate flag	none	0.0
	level 7: bin description parameters		
BINUNIT	bin unit scale selector	none	1.0
LMAX	maximum channel length	m	1.0
LMIN	minimum channel length	m	0.0
WMAX	maximum channel width	m	1.0
WMIN	minimum channel width	m	0.0
	level 7: DC parameters		
A0	bulk charge effect coefficient for channel length	none	1.0
A1	first non-saturation effect parameter	1/V	0.0
A2	second non-saturation factor	none	1.0
AGS	gate-bias coefficient of Abulk	1/V	0.0
ALPHA0	first parameter of impact-ionization current	m/V	0.0
B0	bulk charge effect coefficient for channel width	m	0.0
B1	bulk charge effect width offset	m	0.0

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
BETA0	second parameter of impact-ionization current	V	30.0
CDSC	drain/source to channel coupling capacitance	F/m^2	2.4E-4
CDSCB	body-bias sensitivity of **CDSC**	F/Vm^2	0.0
CDSCD	drain-bias sensitivity of **CDSC**	F/Vm^2	0.0
CIT	interface trap capacitance	F/m^2	0.0
DELTA	effective Vds parameter	V	0.01
DROUT	L-dependence coefficient of the DIBL correction parameter in Rout	none	0.56
DSUB	**DIBL** coefficient exponent in subthreshold region	none	**DROUT**
DVT0	first coefficient of short-channel effect on threshold voltage	none	2.2
DVT0W	first coefficient of narrow-width effect on threshold voltage for small-channel length	1/m	0.0
DVT1	second coefficient of short-channel effect on threshold voltage	none	0.53
DVT2	body-bias coefficient of short-channel effect on threshold voltage	1/V	-0.032
DVT1W	second coefficient of narrow-width effect on threshold voltage for small channel length	1/m	5.3E6
DVT2W	body-bias coefficient of narrow-width effect for small channel length	1/V	-0.032
DWB	coefficient of substrate body bias dependence of Weff	$m/V^{1/2}$	0.0
DWG	coefficient of gate dependence of Weff	m/V	0.0
ETA0	DIBL coefficient in subthreshold region	none	0.08
ETAB	body-bias coefficient for the subthreshold DIBL effect	1/V	-0.07
JS	source-drain junction saturation current per unit area	A/m^2	1.0E-4
JSW	sidewall saturation current per unit length	A/m	0.0
K1	first-order body effect coefficient	$V^{1/2}$	0.5 see page 182
K2	second-order body effect coefficient	none	0.0 see page 182
K3	narrow width coefficient	none	80.0

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
K3B	body effect coefficient of **K3**	1/V	0.0
KETA	body-bias coefficient of bulk charge effect	1/V	-0.047
LINT	length offset fitting parameter from I-V without bias	m	0.0
NFACTOR	subthreshold swing factor	none	1.0
NGATE	poly gate doping concentration	cm^{-3}	0.0
NLX	lateral non-uniform doping parameter	m	1.74E-7
PCLM	channel length modulation parameter	none	1.3
PDIBLC1	first output resistance DIBL effect correction parameter	none	0.39
PDIBLC2	second output resistance DIBL effect correction parameter	none	0.0086
PDIBLCB	body effect coefficient of DIBL correction parameter	1/V	0.0
PRWB	body effect coefficient of **RDSW**	$1/V^{1/2}$	0.0
PRWG	gate-bias effect coefficient of **RDSW**	1/V	0.0
PSCBE1	first substrate current body effect parameter	V/m	4.24E8
PSCBE2	second substrate current body effect parameter	V/m	1.0E-5
PVAG	gate dependence of Early voltage	none	0.0
RDSW	parasitic resistance per unit width	Ω-μm^{WR}	0.0
RSH	source-drain sheet resistance	Ω/square	0.0
U0	mobility at Temp=**TNOM** NMOS PMOS	 670.0 250.0	$cm^2/(V \cdot sec)$
UA	first-order mobility degradation coefficient	m/V	2.25E-9
UB	second-order mobility degradation coefficient	$(m/V)^2$	5.87E-19
UC	body effect of mobility degradation coefficient	m/V^2 1/V	-4.65E-11 when **MOBMOD**=1 or 2 -0.046 when **MOBMOD**=3
VBM	maximum applied body-bias in threshold voltage calculation	V	-3.0
VOFF	offset voltage in the subthreshold region at large W and L	V	-0.08

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
VSAT	saturation velocity at Temp=**TNOM**	m/sec	8.0E 4
VTH0	threshold voltage@Vbs=0 for large L	V	0.7 (NMOS) -0.7 (PMOS) see page 181
W0	narrow-width parameter	m	2.5E-6
WINT	width-offset fitting parameter from I-V without bias	m	0.0
WR	width-offset from Weff for Rds calculation	none	1.0
	Level 7: flicker noise parameters		
AF	frequency exponent	none	1.0
EF	flicker exponent	none	1.0
EM	saturation field	V/m	4.1E7
KF	flicker noise parameter	none	0.0
NOIA	noise parameter A	none	1.0E20 (NMOS) 9.9E18 (PMOS)
NOIB	noise parameter B	none	5.0E4 (NMOS) 2.4E3 (PMOS)
NOIC	noise parameter C	none	-1.4E-12(NMOS) 1.4E-12 (PMOS)
	level 7: NQS parameter		
ELM	Elmore constant of the channel	none	5.0
	level 7: process parameters		
GAMMA1	body effect coefficient near the surface	$V^{1/2}$	see page 182
GAMMA2	body effect coefficient in the bulk	$V^{1/2}$	see page 182
NCH	channel doping concentration	$1/cm^3$	1.7E17
NSUB	substrate doping concentration	$1/cm^3$	6.0E16
TOX	gate-oxide thickness	m	1.5E-8
VBX	Vbs at which the depletion region = **XT**	V	see page 182
XJ	junction depth	m	1.5E-7
XT	doping depth	m	1.55E-7
	level 7: temperature parameters		
AT	temperature coefficient for saturation velocity	m/sec	3.3E4

MOSFET model parameters (continued)

Parameter*	Description	Unit	Default
KT1	temperature coefficient for threshold voltage	V	-0.11
KT1L	channel length dependence of the temperature coefficient for threshold voltage	V*m	0.0
KT2	body-bias coefficient of threshold voltage temperature effect	none	0.022
NJ	emission coefficient of junction	none	1.0
PRT	temperature coefficient for **RDSW**	Ω-μm	0.0
TNOM	temperature at which parameters are extracted	°C	27.0
UA1	temperature coefficient for **UA**	m/V	4.31E-9
UB1	temperature coefficient for **UB**	$(m/V)^2$	-7.61E-18
UC1	temperature coefficient for **UC**	m/V^2	-5.6E -11 when **MOBMOD**=1 or 2
		1/V	-0.056 when **MOBMOD**=3
UTE	mobility temperature exponent	none	-1.5
XTI	junction current temperature exponent coefficient	none	3.0
	level 7: W and L parameters		
LL	coefficient of length dependence for length offset	m^{LLN}	0.0
LLN	power of length dependence for length offset	none	1.0
LW	coefficient of width dependence for length offset	m^{LWN}	0.0
LWL	coefficient of length and width cross term for length offset	$m^{LWN+LLN}$	0.0
LWN	power of width dependence for length offset	none	1.0
WL	coefficient of length dependence for width offset	m^{WLN}	0.0
WLN	power of length dependence of width offset	none	1.0
WW	coefficient of width dependence for width offset	m^{WWN}	0.0
WWL	coefficient of length and width cross term for width offset	$m^{WWN+WLN}$	0.0
WWN	power of width dependence of width offset	none	1.0

* See .MODEL (model definition).

**A ζ in the Default column indicates that the parameter may have corresponding parameters exhibiting length and width dependence. See Model level 4.

† For information on **T_MEASURED**, **T_ABS**, **T_REL_GLOBAL**, and **T_REL_LOCAL**, see .MODEL (model definition).

MOSFET Equations

These equations describe an N-channel MOSFET. For P-channel devices, reverse the signs of all voltages and currents.

In the following equations:

Vbs	= intrinsic substrate-intrinsic source voltage
Vbd	= intrinsic substrate-intrinsic drain voltage
Vds	= intrinsic drain-intrinsic source voltage
Vdsat	= saturation voltage
Vgs	= intrinsic gate-intrinsic source voltage
Vgd	= intrinsic gate-intrinsic drain voltage
Vt	= k·T/q (thermal voltage)
Vth	= threshold voltage
C_{ox}	= the gate oxide capacitance per unit area.
f	= noise frequency
k	= Boltzmann's constant
q	= electron charge
Leff	= effective channel length
Weff	= effective channel width
T	= analysis temperature (°K)
Tnom	= nominal temperature (set using TNOM option)

Other variables are from **MOSFET model parameters**.

Positive current is current flowing into a terminal (for example, positive drain current flows from the drain through the channel to the source).

MOSFET equations for DC current

all levels

Ig = gate current = 0

Ib = bulk current = Ibs+Ibd

where

Ibs = bulk-source leakage current = Iss·($e^{Vbs/(N·Vt)}$-1)

Ibd = bulk-drain leakage current = Ids·($e^{Vbd/(N·Vt)}$-1)

where
if
JS = 0, or AS = 0, or AD = 0

then
Iss = IS
Ids = IS

else
Iss = AS·**JS** + PS·**JSSW**
Ids = AD·**JS** + PD·**JSSW**

Id = drain current = Idrain-Ibd

Is = source current = -Idrain-Ibs

level 1: Idrain

Normal mode: Vds > 0

Case 1

for cutoff region: Vgs-V_{to} < 0

then: Idrain = 0

Case 2

for linear region: Vds < Vgs-V_{to}

then: Idrain = (W/L)·(**KP**/2)·(1+**LAMBDA**·Vds)·Vds·(2·(Vgs-V_{to})-Vds)

Case 3

for saturation region: 0 ≤ Vgs-V_{to} ≤ Vds

then: Idrain = (W/L)·(**KP**/2)·(1+**LAMBDA**·Vds)·(Vgs-V_{to})^2

where
V_{to} = **VTO+GAMMA**·((**PHI**-Vbs)$^{1/2}$-**PHI**$^{1/2}$)

Inverted mode: Vds < 0

Switch the source and drain in the normal mode equations above.

Levels 2 and 3: Idrain

See reference [2] of **References** for detailed information.

MOSFET equations for capacitance

All capacitances are between terminals of the intrinsic MOSFET, in other words, to the inside of the ohmic drain and source resistances. For levels 1, 2, and 3, the capacitance model has been changed to conserve charge.

levels 1, 2, and 3

Cbs = bulk-source capacitance = area cap. + sidewall cap. + transit time cap.

Cbd = bulk-drain capacitance = area cap. + sidewall cap. + transit time cap.

where
if
CBS = 0 *AND* **CBD** = 0

then
Cbs = AS·**CJ**·Cbsj + PS·**CJSW**·Cbss + **TT**·Gbs
Cbd = AD·**CJ**·Cbdj + PD·**CJSW**·Cbds + **TT**·Gds

else
Cbs = **CBS**·Cbsj + PS·**CJSW**·Cbss + **TT**·Gbs
Cbd = **CBD**·Cbdj + PD·**CJSW**·Cbds + **TT**·Gds
where
Gbs = DC bulk-source conductance = dIbs/dVbs
Gbd = DC bulk-drain conductance = dIbd/dVbd

if
Vbs ≤ **FC**·**PB**

then
Cbsj = (1-Vbs/**PB**)$^{-MJ}$
Cbss = (1-Vbs/**PBSW**)$^{-MJSW}$

if
Vbs > **FC**·**PB**

then
Cbsj = (1-**FC**)$^{-(1+MJ)}$·(1-**FC**·(1+**MJ**)+**MJ**·Vbs/**PB**)
Cbss = (1-**FC**)$^{-(1+MJSW)}$·(1-**FC**·(1+**MJSW**)+**MJSW**·Vbs/**PBSW**)

if
Vbd ≤ **FC**·**PB**

then
Cbdj = (1-Vbd/**PB**)$^{-MJ}$
Cbds = (1-Vbd/**PBSW**)$^{-MJSW}$

if
Vbd > **FC**·**PB**

then
Cbdj = (1-**FC**)$^{-(1+MJ)}$·(1-**FC**·(1+**MJ**)+**MJ**·Vbd/**PB**)
Cbds = (1-**FC**)$^{-(1+MJSW)}$·(1-**FC**·(1+**MJSW**))

Cgs = gate-source overlap capacitance = **CGSO**·W

Cgd = gate-drain overlap capacitance = **CGDO**·W

Cgb = gate-bulk overlap capacitance = **CGBO**·L

levels 4 and 6

See references [6] and [7] of References.

MOSFET equations for temperature effects

The ohmic (parasitic) resistances have no temperature dependence.

all levels

IS(T) = **IS**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/Vt}$

JS(T) = **JS**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/Vt}$

JSSW(T) = **JSSW**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/Vt}$

PB(T) = **PB**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

PBSW(T) = **PBSW**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

PHI(T) = **PHI**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

where
Eg(T) = silicon bandgap energy = 1.16 - .000702·T^2/(T+1108)

CBD(T) = **CBD**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CBS(T) = **CBS**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CJ(T) = **CJ**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CJSW(T) = **CJSW**·(1+**MJSW**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

KP(T) = **KP**·$(T/Tnom)^{-3/2}$

UO(T) = **UO**·$(T/Tnom)^{-3/2}$

MUS(T) = **MUS**·$(T/Tnom)^{-3/2}$

MUZ() = **MUZ**·$(T/Tnom)^{-3/2}$

X3MS(T) = **X3MS**·$(T/Tnom)^{-3/2}$

MOSFET equations for noise

Noise is calculated assuming a 1.0-hertz bandwidth, using the following spectral power densities (per unit bandwidth).

The model parameter **NLEV** is used to select the form of shot and flicker noise, and **GDSNOI** is the channel shot noise coefficient model parameter. When **NLEV**<3, the original SPICE2 shot noise equation is used in both the linear and saturation regions, but the use of this equation may produce inaccurate results in the linear region. When **NLEV**=3, a different equation is used that is valid in both linear and saturation regions.

The model parameters **AF** and **KF** are used in the small-signal AC noise analysis to determine the equivalent MOSFET flicker noise.

For more information, see reference [5] of References.

MOSFET channel shot and flicker noise

$$Ichan^2 = Ishot^2 + Iflick^2$$

intrinsic MOSFET flicker noise

for **NLEV** = 0

$$Iflick^2 = \frac{\mathbf{KF} \cdot Idrain^{\mathbf{AF}}}{COX \cdot Leff^2 \cdot f}$$

for **NLEV** = 1

$$Iflick^2 = \frac{\mathbf{KF} \cdot Idrain^{\mathbf{AF}}}{COX \cdot Weff \cdot Leff \cdot f}$$

for **NLEV** = 2, **NLEV** = 3

$$Iflick^2 = \frac{\mathbf{KF} \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{\mathbf{AF}}}$$

intrinsic MOSFET shot noise

for **NLEV** < 3

$$Ishot^2 = \frac{8 \cdot k \cdot T \cdot gm}{3}$$

for **NLEV** = 3

$$Ishot^2 \equiv \frac{8 \cdot k \cdot T}{3} \times \beta \times (Vgs - Vth) \frac{1 + a + a^2}{1 + a} \times \mathbf{GDSNOI}$$

where
for linear region:
$a = 1 - (Vds/Vdsat)$
for saturation region:
$a = 0$

parasitic resistance thermal noise

RD $Id^2 = 4 \cdot k \cdot T/RD$

RG $Ig^2 = 4 \cdot k \cdot T/RG$

RS $Is^2 = 4 \cdot k \cdot T/RS$

RB $Ib^2 = 4 \cdot k \cdot T/RB$

References

For a more complete description of the MOSFET models, refer to:

[1] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," IEEE Journal of Solid-State Circuits, SC-3, 285, September 1968.

[2] A. Vladimirescu, and S. Lui, "The Simulation of MOS Integrated Circuits Using SPICE2," Memorandum No. M80/7, February 1980.

[3] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors," IEEE Journal of Solid-State Circuits, SC-22, 558-566, August 1987.

[4] J. R. Pierret, "A MOS Parameter Extraction Program for the BSIM Model," Memorandum No. M84/99 and M84/100, November 1984.]

[5] P. Antognetti and G. Massobrio, Semiconductor Device Modeling with SPICE, McGraw-Hill, 1993.

[6] Ping Yang, Berton Epler, and Pallab K. Chatterjee, "An Investigation of the Charge Conservation Problem for MOSFET Circuit Simulation," IEEE Journal of Solid-State Circuits, Vol. SC-18, No.1, February 1983.

[7] J.H. Huang, Z.H. Liu, M.C. Jeng, K. Hui, M. Chan, P.K. KO, and C. Hu, "BSIM3 Manual," Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720.

[8] Department of Electrical Engineering and Computer Science, "BSIM3v3.1 Manual," University of California, Berkeley, CA 94720.

[9] J. C. Bowers, and H. A. Neinhaus, SPICE2 Computer Models for HEXFETs, Application Note 954A, reprinted in HEXFET Power MOSFET Databook, International Rectifier Corporation #HDB-3.

[10]M.Bucher,C.Lallement,C.Enz,F.Theodoloz,F.Krummenacher.TheEPFL–EKVMOSFET Model Equations for Simulation Technical Report: Model Version 2.6. Electonics Laboratories, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland. Updated September, 1997.

For more information on References [2] and [4], contact:

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