Voltage-Mode Buck Regulators
Voltage-Mode Regulator
Voltage Mode - Advantages and Disadvantages

• Advantages

1. Stable modulation/less sensitive to noise
2. Single feedback path
3. Can work over a wide range of duty cycles

• Disadvantages

1. Loop gain proportional to $V_{IN}$
2. LC double pole often drives Type III compensation
3. CCM and DCM differences - a compensation challenge
4. Slow response to input voltage changes
5. Current limiting must be done separately
Voltage Mode - Modulator Gain

\[ A_M = \frac{V_{IN}}{V_P} \]
Voltage Mode - Output Filter

\[ \frac{V_{\text{OUT}}}{V_{\text{SW}}} = \frac{Z_B}{Z_A + Z_B} \]

*(Rx, Cy) indicate the components that drive the locations of the pole and the zero, detailed equations are in the notes.*
The easiest place to compensate the entire loop is to adjust the compensation around the error amplifier. Several different approaches are possible.
Voltage Mode - Type II Compensation

\[ \frac{V_C}{V_{OUT}} = - \frac{Z_F}{Z_I} \]

* (Rx, Cy) indicate the components that drive the locations of the pole and the zero
Voltage Mode - Type III Compensation

\[ \frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I} \]

*(R_x, C_y) indicate the components that drive the locations of the poles and zeros,*
Current-Mode Buck Regulators
Current-Mode Buck-Regulator Architecture

Modulator and Power Stage

Corrective Ramp

PWM Comparator

Current Sense Amplifier

Modulator and Power Stage

Integrated or external

Feedback, Error Amplifier, and Compensation

Reference

A(s)

A(s)

V_{OUT}

V_{OUT}

V_{IN}

V_{IN}

V_{C}

V_{C}

L

C

R_{L}

R_{C (ESR)}
Current Mode - Advantages and Disadvantages

• **Advantages**
  1. Power plant gain offers a single-pole roll-off
  2. Line rejection
  3. Cycle-by-cycle current limiting protection
  4. Current sharing

• **Disadvantages**
  1. Noise
  2. Minimum ON-time
  3. Current Probe (Rsense, LEM, …)
CMC Sub Harmonic Oscillation

\[ D = 0.6 \]

\[ D = 0.33 \]
Slope Compensation

\[ m_C = \text{Internal Slope Comp} \]

Stability criteria

\[ 1 > \frac{m_2 - m_C}{m_1 + m_C} \]
Current Mode - Output Filter

\[ \omega_{z1} = \frac{1}{C_{OUT} R_{ESR}} \]

\[ \omega_{p1} = \frac{1}{C_{OUT} R_{LOAD}} + \frac{1}{f_s L C_{OUT}} (m_z D' - 0.5) \]
Current Mode - Error Amplifier

Compensation components internal in some devices

\[ A_{FB} = \frac{R_{fb2}}{R_{fb1} + R_{fb2}} = \frac{V_{FB}}{V_{out}} \]

\[ \omega_{z2} = \frac{1}{C_{C1}R_{C1}} \]

\[ \omega_{p2} = \frac{1}{C_{C1}R_{OUT}} \]

\[ A_{EA} = g_{m}R_{OUT} \]
Current Mode – Control Loop Gain

\[ T = A_{DC} \]

\[ A_{DC} = A_{CM} A_{EA} A_{FB} \]

Output Filter Pole

Output Filter Zero

EA Pole

EA Zero

Complex Pole @ Fsw/2

\[ Q = \frac{1}{\pi \left( \frac{m_c}{m_1} + \frac{1}{2} - D \right)} \]
Current-Mode Load Transients – Performance Tradeoffs

• Current mode control behaves like a current source driving the output capacitor

• The output impedance of a closed loop system is:

\[
Z_{OUT\_CLOSED\_LOOP} = \frac{Z_{OUT\_OPEN\_LOOP}}{1 + \text{Loop\_Gain}}
\]

\[
\Delta V_{OUT} = Z_{OUT}\Delta I_{OUT}
\]

• Rule of thumb for high frequency load transients (\(t_{SLEW} \leq 1/f_{CROSSOVER}\)):
Peak versus Average Current Mode Control
Current Mode Control [CMC]

• **Disadvantages of Peak CMC**
  1. Poor Noise Immunity (at switching on)
  2. Slope Compensation required when D > 0.5
  3. Peak to Average current error (ok when ripple <<)
  4. Topology problem when $i_L \neq i_{out}$

• **Advantages of Average CMC**
  1. Average Current Tracks well the Current Program in CCM or DCM. Voltage loop control is oblivious.
  2. Slope Compensation not required but loop gain @ Fsw is limited to achieve stability
  3. Noise Immunity is Excellent even at low Ic (set point)
  4. ACMC is ok whatever the topology ($i_L \neq i_{out}$) is.
Buck ACMC design example

Switching Frequency, $f_S = 100$ kHz
Input Voltage, $V_{IN} = 15 - 30$V
Output Voltage, $V_o = 12$V
Output Current, $I_o = 5$A (6A O.L.)
Inductance, $L = 60 \ \mu$H
max. $\Delta I_o \ @ \ 30$V (100 kHz) = 1.2A
Sense Resistance, $R_S = 0.10$
Control Loop Gain at Fsw

The amplified current down slope \( V_{ca} \) on the PWM comparator must be smaller than the Oscillator ramp up slope

\[ \Leftrightarrow \]

Current Amplifier Gain \( @ F_{crossover} < G_{stability} \)

\[
(V_o/L)R_s G_{CA} = V_s f_s
\]
Buck ACMC design example

\[ \begin{align*}
\therefore \quad \max G_{CA} &= \frac{\varphi_{CA}}{\varphi_{RS}} = \frac{V_S f_S L}{V_o R_S} \quad (1) \\
\frac{\varphi_{RS}}{\varphi_{CA}} &= \frac{R_S}{V_S} \frac{V_{IN}}{sL} = \frac{1590}{f} \quad (@30V) \quad (2)
\end{align*} \]

\[ \begin{align*}
\frac{R_S}{V_S} \frac{V_{IN}}{2\pi f_C L} \frac{V_S f_S L}{V_o R_S} &= 1 \\
f_C &= \frac{f_S V_{IN}}{2\pi V_o} = \frac{f_S}{2\pi D} \quad (3)
\end{align*} \]
Buck ACDC design example