Grounding and earthing

Véronique Beauvois, Ir.
2018-2019
Grounding and earthing

General definition:
- Earth’s ground considered for electrical installations as a reference of 0V
- Variable electrical conductivity – naturally electrical currents are flowing.

Key-roles:
- Lightning current flowing
- Leakage current flowing
- Protection of persons

(IEC 364 – Electrical Installations of Buildings & IEC 50164 – Lightning protection components)
Earthing/grounding and EMC:
For a lot of EMC phenomena (transient disturbances, HF currents…), earthing conductors are not efficient as they are very long and the used topology means a high impedance versus HF. The only solution is meshing to get equipotentiality.
Mesh size: $\pm \lambda/10$.
All electrical elements, components, should be connected as shielding, screens, CM connections of filters (remember some remarks on good implementation in Components).
Grounding and earthing

Loop between grounding = surface between 2 grounding cables, resulting of a systematic meshing of ground to insure equipotentiality.
Solution?
To reduce loop size with a small mesh size.
Grounding loop: surface loop between a power/signal cable and a corresponding grounding cable.
Solution? To reduce loop size with a very short distance between power/signal cable and corresponding grounding cable (all along the cables).
Grounding and earthing

Star grounding

Series grounding

Câbles de terre inévitablement longs

Conducteur de protection (PE)

Lmax 50cm
Grounding and earthing

Boucles de masse de grande surface

Forte impédance commune

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**Building:**
- ground meshing by level
- connect all metallic structures of building to the ground (pipes, ducts, duckboards…)
- in sensitive zone (computers, data, measurements), consider a small meshed system

**Equipment:**
- Connect all metallic structures together

**Rack:**
- a metal plate in the bottom of the rack
- insulating coating and painting
- good contact between components and metal plate (green-yellow cabling is not sufficient for EMC).
Grounding and earthing
Shielding

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A variable electric field and a infinite conducting wall, will induce currents in the wall. These currents will generate a reflected E-field in opposite direction. This is necessary to comply with limit condition $E=0$ on the wall. The amplitude of the reflected wave determines the **loss by reflection**. As the wall has a finite conductivity, a part of the current penetrates the wall and a part of this current will be present on the other side of the wall, emitting its own wave. $E_{\text{incident}}$ over $E_{\text{transmitted}}$ defines the **shielding efficiency**. The thickness of the wall influences the attenuation of the current. **Loss by absorption** depends of the number of skin depths in the wall thickness.


E_i/E_t > S.E. = 20 \log (E_i/E_t) (dB)
**Shielding**

Skin depth represents the property to limit the current at the internal surface of a conductor. It decreases when: frequency increases, conductivity increases and permeability increases. At each skin depth, $E$ is decreased by $\frac{1}{e}$ or 8.6 dB. e.g. aluminium, skin depth is 0.015 mm @ 30 MHz.

In the case of high frequencies, very thin conductors are efficient for shielding.
Loss by reflection

These losses are related to the ratio of wave impedance (E/H, in far-field conditions 377 Ω) and impedance of the wall (frequency, conductivity and permeability).

For a good conductor (copper, aluminium), losses by reflection are important.

If frequency increases, losses are decreasing for E and increasing for H.

Plane wave: \( R = 168 - 10 \log_{10} \left( \frac{\mu_r}{\sigma_r} . f \right) \) dB

E-field: \( R_E = 322 - 10 \log_{10} \left( \frac{\mu_r}{\sigma_r} . f^3 . r^2 \right) \) dB

H-field: \( R_H = 14.6 - 10 \log_{10} \left( \frac{\mu_r}{\sigma_r} . f . r^2 \right) \) dB
Loss by absorption
As already mentioned those losses depend of the wall thickness and skin depth, depending of material properties.
If thickness is constant, steel is better than copper regarding those losses.
At high frequency, this is the major part of losses, they are increasing as the square of frequency.
\[ A = 20 \log\left(\frac{E_0}{E_1}\right) = 20 \log e^{t/\delta} = 20.(t/\delta).\log e = 8.69.\,(t/\delta) \, dB \]
Where \( t \) is the thickness of the wall and \( \delta \) the skin depth.
Shielding

**Shielding efficiency**
The ratio between field without wall and field with wall.

This is the sum of 3 losses:
SE (dB) = R(dB) + A(dB) + B(dB)

- R : reflection losses (E,H)
- A : absorption losses
- B : contribution of multiple reflections and transmissions inside the wall.
Shielding

Different kind of envelops:
- completely conductive (rack, drawer, box);
- metallic structure with insulating panels;
- completely insulating material.

For insulating material, some treatments exist to add a conductive coating.
We have already mentioned that it is efficient in high frequency.
Solutions:
- Conductive painting
- Spraying fusion metal
- Metal film deposit
- Vaporisation under vacuum conditions
Solutions:
- Doors and panels separation
  - Distance between 2 fixations (screws…)
  - Increasing the number of fixations (screws, different sorts of gaskets)
- Contact surfaces to clean: no painting…
Shielding

Médiocre

Meilleur

Supérieur
(effet de cheminée si $t \geq l$)

Nid d'abeille

Mousse métallique

Plaque de surépaisseur soudée

à monter sur la paroi avec un joint conducteur performant

Nid d'abeille, pour efficacité de blindage $E_B > 80$ dB
Cabling:

- Not shielded cables: filters
- Shielded cables: connections of shielding with structure, walls
- Non electric “cables”: waveguide for non metallic ducts, good connection for metallic ducts
Design rules

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Design rules

Grounding/earthing in racks - connections

PE - PEN

Fil vert / Jaune

L / I < 3

Rondelle

Boulon
Design rules
Design rules
Design rules

Power supplies management

Transformateur

Equipment perturbateur  Equipment sensible  NON RECOMMANDE

Equipment perturbateur  Equipment sensible  PREFERABLE

Equipment perturbateur  Equipment sensible  EXCELLENT

[EN 50174-2]
Design rules
Design rules
Design rules
 mauvais :

angles d'intersections quelconques

nombreuses boucles

courants faibles et courants forts mélangés

bon :

angles droits

boucles de surfaces minimales

courants faibles et courants forts séparés (éventuellement par une séparation métallique)
Design rules

Cabling rules

- Equipotentiality of grounding (LF & HF) is ensured
- Do not use sensitive signals and disturbing signals in the same cable

- Reduce the parallel length of sensitive signals cables and disturbing signals cable
- Shielded cables permits those signals cables in the same duct.
Design rules

Câbles de puissance

Fils de contrôle-commande

Conducteurs de mesure avec écran

\[ d = \text{quelques centimètres} \]
Design rules

Cabling rules

- Keep distance between sensitive cables and disturbing cables (costless and efficient solution) – this distance increases with the length of parallel cables.
- Reduce grounding loop surfaces
Design rules

Cabling rules

- Signal conductor near grounding conductor

* : capteurs bas niveau ==> classe 2
Design rules

Cabling rules
Design rules

Cabling rules

- Any unused conductor should be connected to ground at both ends
Design rules

Cabling rules

- Shielding connections?
  - at both ends?
    - very efficient against external HF disturbances
    - no voltage between cable and ground
Design rules

Cabling rules

- Shielding connections?
  - at 1 end?
    - not efficient against external HF disturbances
    - to delete low frequency signals in shielding called « ronflette »

Protection BF
Design rules

Cabling rules

Protection HF + BF
Design rules

Cabling rules

- Shielding connections?
  - not connected?
    - FORBIDDEN if accessible to touch (voltage between shielding and ground)
  - not efficient against external HF disturbances
Design rules

Cabling rules
Design rules
Cabling rules

[EN 50174-2]
Design rules

Cabling rules

Goulottes
- Câble sensible
  - Moyen
  - Excellent

Cornières
- Déconseillé
  - Bien
  - Excellent
Design rules
Cabling rules

[EN 50174-2]
Design rules
For electronic circuits and PCBs

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2018-2019
Why?

- Frequency is increasing (wireless, Bluetooth)
- Speed is increasing (clock, Mbit/sec)
- $t_r$ and $t_f$ are decreasing
- Components density is increasing (SMD)
- Tracks density /cm$^2$ is increasing

Broadband spectrum interferences
PCB design (PCB design software!)
Circuit design and grounding

Protections classification:
- Primary: circuit design (decoupling, balanced configuration, speed and bandwidth limitations)- PCB design and grounding,
- Secondary: external circuit interfaces, cabling (filtering), connectors,
- Tertiary: full shielding (cost)
1st step: to take care of the division of the circuit

<table>
<thead>
<tr>
<th>Dig. 1</th>
<th>Supply</th>
<th>An. 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>An. 1</td>
<td>I/O</td>
<td>Dig. 2</td>
</tr>
</tbody>
</table>

To spot critical zones:
- sources
  (µP, video…)
- victims
  (low level analogue…)

Different ports are all over the perimeter – shielding and ports filtering
Divided circuit
2nd step: Grounding

- do not confuse ground and earth (PE)
- grounding role: to give a reference for all connections
- low impedance track to send the current to the source
- low transfer impedance solutions
a) To suppress common grounding Z (OK up to some MHz, then $C_p$ et $U_{CM}$ due to length of links)

b) Similar circuits linked together, noisy circuits near grounding point.

c) A lot of short connections (<$0.1\lambda$) for digital circuits.
- 1 PCB side/ 1 side versus 2 sides
- Multi-layer PCB (ground plane)
- Reduce impedance
- Grounding track // and near signal track
- Grounding: grid or ground plane
- SMD (to reduce loop surface, length, PCB size)
- ...

...
Track impedance

circuit équivalent d'une piste de cuivre de 35 microns, longueur 10 cm, largeur 0,5 mm

<table>
<thead>
<tr>
<th>Inductance approx. à 30 MHz</th>
<th>Impédance à 30 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 nH</td>
<td>11,3 Ω</td>
</tr>
<tr>
<td>30 nH</td>
<td>5,6 Ω</td>
</tr>
<tr>
<td>16 nH</td>
<td>3,0 Ω</td>
</tr>
<tr>
<td>18 nH</td>
<td>3,4 Ω</td>
</tr>
<tr>
<td>2 mm</td>
<td>5,9</td>
</tr>
</tbody>
</table>
Grid or meshed grounding

The number of return path for current to ground should be important to reduce L.
Tracks with width $\gg$

The comb configuration is not a good solution.
5.13

S détermine dans tous les cas l'inductance globale de la boucle

pistes parallèles

pistes de part et d'autre de la platine

plan de masse sur la face opposée de la platine, offre un chemin de retour à toute piste de l'autre côté
- Do not interrupt ground plane.
- If this interruption is mandatory, add a bridge (as short as possible and near the critical track).
- No slot in the ground plane (multi-layer is ideal).
Design rules
For electronic circuits and PCBs
(part II)

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2018-2019
Interference sources on PCBs

- Studies have shown that VLSI devices (processor, DDR memories, FPGA) are too small to act as direct sources of radiated EMI but,
- EMI noise is generated by:
  - coupling to heatsink,
  - coupling to traces,
  - coupling to reference plane.
Interference sources on PCBs

- Common-impedance coupling through power supplies,
- Common-impedance coupling through return conductor,
- Mismatch on transmission lines -> reflexions,
- Crosstalk between adjacent conductors,
- Coupling in low level, high gain amplifiers,
- Transients from inductive load switching, coupling to adjacent circuits,
- Power supply generated noise.

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"Grounding" on PCBs

- What are the functions of “grounding” on a PCB?
  - **Signal return path.** For each high speed digital signal, a current goes from the source to the destination, the return current need a path that is provided by the ground.
  - **DC power return path.** Power supply current goes back to the power supply through the ground plane.
  - **Image plane.** By providing a ground plane close to signal layers, the ground plane provides an image plane that allows image currents to flow, therefore reducing EMI.
Return path discontinuities on PCBs

- Trace crosses a gap or split in the plane without adequate provision for its return current
- Trace much too close to a via hole's antipad
- Insufficient spacing between the two via holes' antipads to route the trace between them
- Trace too close to a gap in the plane
- Layer 2: Reference plane Carrying the return current for the traces on layer 1
- Layer 1: Signal or Power Trace
- Trace leaves the plane without adequate provision for its return current
Design rules
For electronic circuits and PCBs
(part III)

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Harm. impaires  Harm. paires et impaires
How to choose the logic family?
$t \longleftrightarrow f$

Graph showing the frequency response of different types of 74 series ICs (74HC244, 74AC244, 74F244, 74F) with a $10\text{MHz}$ signal. The graph indicates the performance in dB over frequency from 10 MHz to 1 GHz.
Radiated emission of circuits

Differential mode
R.E.

Common mode
R.E.

Table 6.1

Table 6.2
Loop = small if dimensions $< \lambda/4$, means 1m @ 75MHz
IC loops could considered as small up to some 100 MHz
Maximum E-field of this loop @ 10 m measurement distance:
$E (V/m) = 263 \times 10^{-12} \times f(MHz)^2 \times A(cm^2) \times I_S (mA) \quad \longrightarrow +40dB/dec$
According to:
\[ E \text{ (V/m)} = 263 \times 10^{-12} \times f(\text{MHz})^2 \times A(\text{cm}^2) \times I_s(\text{mA}) \quad \text{---}> 40 \text{ dB/dec} \]

Question: this PCB needs or not an additional shielding?
A=10 cm²; Is=20 mA and f=50 MHz
E=42 dBµV/m means 12dB over the limit in class B
So if current I and frequency f are fixed, A could not be reduced, a shielding is necessary.
dynamic commutation current / component to charge or discharge the capacitor

Limit EN 55022 cl.B

Table 6.1 – Émission en mode différentiel : surface maximale permise.
E (V/m) = 1.26 \times 10^{-4} \times f(MHz) \times L(m) \times I_{MC} (mA)

if the cable is represented by a short monopole (L<\lambda/4) @ 10m of the ground

e.g. 1m of cabling, E=42dB\mu V/m, then Is=20\mu A (/1000#I_{MD})
C.M. ----> R.E. of PCB

CM voltage to cable, ΔI on ground path
Differential noise voltage $V_N = \Delta I j\omega L$ (between reference ground and cable connection)
$Z \approx 150\Omega$ (constant with f)
<table>
<thead>
<tr>
<th>Famille logique</th>
<th>t\textsubscript{\text{o}}</th>
<th>I\textsubscript{\text{o}}</th>
<th>Δf</th>
<th>Longueur de piste en cm : fréquence d’horloge</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ns</td>
<td>mA</td>
<td></td>
<td>4 MHz</td>
</tr>
<tr>
<td>4000B CMOS à 5 V</td>
<td>40</td>
<td>6</td>
<td></td>
<td>180</td>
</tr>
<tr>
<td>74HC</td>
<td>6</td>
<td>20</td>
<td></td>
<td>8,5</td>
</tr>
<tr>
<td>74LS</td>
<td>6</td>
<td>50</td>
<td></td>
<td>3,25</td>
</tr>
<tr>
<td>74ALS</td>
<td>3,5</td>
<td>50</td>
<td></td>
<td>1,9</td>
</tr>
<tr>
<td>74AC</td>
<td>3</td>
<td>80</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>74F</td>
<td>3</td>
<td>80</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>74AS</td>
<td>1,4</td>
<td>120</td>
<td></td>
<td>0,4</td>
</tr>
</tbody>
</table>

Longueur de piste autorisée pour 30 dBμV/m 30 MHz - 230 MHz, 37 dBμV/m 230 MHz - 1000 MHz à 10 m ; longueur du câble = 1 m ; agencement : pistes parallèles de 0,5 mm distantes de 0,5 mm (2,8 nH/cm).

Utilisation : prenons par exemple la famille 74HC avec $F_{ck} = 10$ MHz. Le cas le plus défavorable est à 90 MHz (9ème harmonique).

À partir de l’équation (4.7), pour une intensité de champ $E$ de 30 dBμV/m et 1 m de câble, $I_{CM}$ doit être égal à 2,8 μA.

Selon $V_N = I_{CM} \times 150$, avec l’atténuation de couplage de 20 dB, $V_N = 4,18$ mV.

L’analyse de Fourier de la source de courant, en utilisant la section C.7 avec $(t + t_f)/T = 0,5$ ; $T = 100$ ns ; $t_f = 6$ ns et $I = 20$ mA, donne 0,826 mA pour $I_{(9)}$, le courant du neuvième harmonique.

Ensuite, suivant $L = V_N/2\pi f(9)$, l’inductance aux bornes de laquelle on peut admettre $V_N$ à $I_{(9)}$ et 90 MHz est de 8,95 nH, soit 3,19 cm autorisés à 2,8 nH/cm.

**Tableau 6.2** – Émissions en mode commun : longueur de piste admissible.
For the same signal in DM or CM trapezoidal @12MHz, with $t_r$ and $t_f$ 3.5ns
CM Ipk 0.1mA in cable, with L 2m
DM 20mA in a loop of 5cm$^2$

$$E (V/m) = 263 \times 10^{-12} \times f(MHz)^2 \times A(cm^2) \times I_S (mA)$$  \text{loop-IC}

$$E (V/m) = 1.26 \times 10^{-4} \times f(MHz) \times L(m) \times I_{MC} (mA)$$  \text{antenna-cable}
R.E. > main source processor clock

Commercial standards: no difference between N.B. and B.B.
- To reduce N.B. with buffer on lines and take care of ground plane.
- To reduce B.B. sources on data lines, video...