Grounding and earthing

Véronique Beauvois, Ir.
2019-2020
Grounding and earthing

General definition:
- Earth’s ground considered for electrical installations as a reference of 0V
- Variable electrical conductivity – naturally electrical currents are flowing.

Key-roles:
- Lightning current flowing
- Leakage current flowing
- Protection of persons

(IEC 364 – Electrical Installations of Buildings & IEC 50164 – Lightning protection components)
Earthing/grounding and EMC: 
For a lot of EMC phenomena (transient disturbances, HF currents...), earthing conductors are not efficient as they are very long and the used topology means a high impedance versus HF.

The only solution is **meshing** to get **equipotentiality**.

Mesh size: $\pm \lambda/10$.

All electrical elements, components, should be connected as shielding, screens, CM connections of filters (remember some remarks on good implementation in *Components*).
Loop between grounding = surface between 2 grounding cables, resulting of a systematic meshing of ground to insure equipotentiality. Solution? To reduce loop size with a small mesh size.
**Grounding loop**: surface loop between a power/signal cable and a corresponding grounding cable.
Solution? To reduce loop size with a very short distance between power/signal cable and corresponding grounding cable (all along the cables).
Grounding and earthing

Câbles de terre inévitablement longs

Star grounding

Lmax 50cm

Conducteur de protection (PE)

Series grounding
Building:
• ground meshing by level
• connect all metallic structures of building to the ground (pipes, ducts, duckboards…)
• in sensitive zone (computers, data, measurements), consider a small meshed system

Equipment:
• Connect all metallic structures together

Rack:
• a metal plate in the bottom of the rack
• insulating coating and painting
• good contact between components and metal plate (green-yellow cabling is not sufficient for EMC).
Grounding and earthing
Shielding

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2019-2020
Shielding

A variable electric field and an infinite conducting wall, will induce currents in the wall. These currents will generate a reflected E-field in opposite direction. This is necessary to comply with limit condition $E=0$ on the wall. The amplitude of the reflected wave determines the loss by reflection. As the wall has a finite conductivity, a part of the current penetrates the wall and a part of this current will be present on the other side of the wall, emitting its own wave. $E_{\text{incident}}$ over $E_{\text{transmitted}}$ defines the shielding efficiency. The thickness of the wall influences the attenuation of the current. Loss by absorption depends on the number of skin depths in the wall thickness.
Shielding

\[ \text{Ei/Et > S.E.} = 20 \log (\text{Ei/Et}) \text{ (dB)} \]
Skin depth represents the property to limit the current at the internal surface of a conductor. It decreases when: frequency increases, conductivity increases, and permeability increases. At each skin depth, E is decreased by 1/e or 8.6 dB. e.g. aluminium, skin depth is 0.015 mm @ 30 MHz.

In the case of high frequencies, very thin conductors are efficient for shielding.
Loss by reflection

These losses are related to the ratio of wave impedance (E/H, in far-field conditions 377 Ω) and impedance of the wall (frequency, conductivity and permeability).

For a good conductor (copper, aluminium), losses by reflection are important.

If frequency increases, losses are decreasing for E and increasing for H.

Plane wave \[ R = 168 - 10 \log_{10} \left( \frac{\mu_r}{\sigma_r} \cdot f \right) \text{ dB} \]

E-field \[ R_E = 322 - 10 \log_{10} \left( \frac{\mu_r}{\sigma_r} \cdot f^3 \cdot r^2 \right) \text{ dB} \]

H-field \[ R_H = 14.6 - 10 \log_{10} \left( \frac{\mu_r}{\sigma_r} \cdot f \cdot r^2 \right) \text{ dB} \]
Loss by absorption
As already mentioned those losses depend of the wall thickness and skin depth, depending of material properties. If thickness is constant, steel is better than copper regarding those losses. At high frequency, this is the major part of losses, they are increasing as the square of frequency.

\[ A = 20 \log\left(\frac{E_0}{E_1}\right) = 20 \log e^{t/\delta} = 20(t/\delta) \log e = 8.69 \ (t/\delta) \text{ dB} \]

Where \( t \) is the thickness of the wall and \( \delta \) the skin depth.
Shielding efficiency
The ratio between field without wall and field with wall.

This is the sum of 3 losses:
\[ SE \ (dB) = R(dB) + A(dB) + B(dB) \]

- **R**: reflection losses (E, H)
- **A**: absorption losses
- **B**: contribution of multiple reflections and transmissions inside the wall.
Different kind of envelopes:
- completely conductive (rack, drawer, box);
- metallic structure with insulating panels;
- completely insulating material.

For insulating material, some treatments exist to add a conductive coating.
We have already mentioned that it is efficient in high frequency.
Shielding

Solutions:
- Conductive painting
- Spraying fusion metal
- Metal film deposit
- Vaporisation under vacuum conditions
Solutions:
- Doors and panels separation
  - Distance between 2 fixings (screws…)
  - Increasing the number of fixings (screws, different sorts of gaskets)
  - Contact surfaces to clean: no painting…
Shielding

Médiocre

Meilleur

Supérieur (effet de cheminée si $t \geq l$)

Nid d’abeille

Mousse métallique

$Nid d’abeille$, pour efficacité de blindage $E_B > 80$ dB

Plaque de surépaisseur soudée

$\text{à monter sur la paroi avec un joint conducteur performant}$
Cabling:

- Not shielded cables: filters
- Shielded cables: connections of shielding with structure, walls
- Non electric “cables”: waveguide for non metallic ducts, good connection for metallic ducts
Design rules
For electrical circuits

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2019-2020
Design rules

Grounding/earthing in racks - connections

PE - PEN

Fil vert / jaune

L < 3

Rondelle

Boulon

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Design rules
Design rules
Design rules

Power supplies management

[EN 50174-2]
Design rules
Design rules
Design rules
 mauvais :
angles d'intersections quelconques
nombreuses boucles
courants faibles et courants forts mélangés

bon :
angles droits
boucles de surfaces minimales
courants faibles et courants forts séparés (éventuellement par une séparation métallique)
Design rules

Cabling rules

- Equipotentiality of grounding (LF & HF) is ensured
- Do not use sensitive signals and disturbing signals in the same cable
- Reduce the parallel length of sensitive signals cables and disturbing signals cable
- Limit cable lengths
- Shielded cables permits those signals cables in the same cable tray.
Design rules

Câbles de puissance

Fils de contrôle-commande

Conducteurs de mesure avec écran

\[ d = \text{quelques centimètres} \]
Design rules
Cabling rules

- Keep distance between sensitive cables and disturbing cables (costless and efficient solution) – this distance increases with the length of parallel cables.
Design rules
Cabling rules

- Reduce grounding loop surfaces
Design rules
Cabling rules

- Signal conductor near grounding conductor

* : capteurs bas niveau ==> classe 2
Design rules

Cabling rules
- Any unused conductor should be connected to ground at both ends
Design rules
Cabling rules

- Shielding connections?
  - at both ends?
    - very efficient against external HF disturbances
    - no voltage between cable and ground
- Shielding connections?
  - at 1 end?
    - not efficient against external HF disturbances
    - to delete low frequency signals in shielding called « ronflette »

![Diagram of shielding connection with protection BF]
Design rules
Cabling rules

Protection HF + BF
Design rules

- Shielding connections?
  - not connected?
  - FORBIDDEN if accessible to touch (voltage between shielding and ground)
  - not efficient against external HF disturbances
Design rules
Cabling rules
Design rules
Cabling rules

[EN 50174-2]
Design rules
Cabling rules

**Goulottes**
- Câble sensible
  - Moyen
  - Excellent

**Cornières**
- Déconseillé
  - Bien
  - Excellent
Design rules

Cabling rules

Non

Non recommandé

Oui

[EN 50174-2]
Design rules
For electronic circuits and PCBs
(part I)

Véronique Beauvois, Ir.
2019-2020
Why?

- Frequency is increasing (wireless, Bluetooth)
- Speed is increasing (clock, Mbit/sec)
- $t_r$ and $t_f$ are decreasing
- Components density is increasing (SMD)
- Tracks density /cm² is increasing

Broadband spectrum interferences
PCB design (PCB design software!)
Circuit design and grounding

Protections classification:
• Primary: circuit design (decoupling, balanced configuration, speed and bandwidth limitations) - PCB design and grounding,
• Secondary: external circuit interfaces, cabling (filtering), connectors,
• Tertiary: full shielding (cost)
Circuit design and grounding

1st step: to take care of the division of the circuit

<table>
<thead>
<tr>
<th>Dig. 1</th>
<th>Supply</th>
<th>An. 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>An. 1</td>
<td>I/O</td>
<td>Dig. 2</td>
</tr>
</tbody>
</table>

Different ports are all over the perimeter – shielding and ports filtering

To spot critical zones:
- Sources (µP, video…)
- Victims (low level analogue…)

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Circuit design and grounding

Divided circuit
Circuit design and grounding

Divided circuit
Circuit design and grounding

2nd step: Grounding

- do not confuse ground and earth (PE)
- grounding role: to give a reference for all connections
- low impedance track to send the current to the source
- low transfer impedance solutions
a) To suppress common grounding $Z$ (OK up to some MHz, then $C_p$ et $U_{CM}$ due to length of links).

b) Similar circuits linked together, noisy circuits near grounding point.

c) A lot of short connections ($<0.1\lambda$) for digital circuits.
Circuit design and grounding

- 1 PCB side/ 1 side versus 2 sides
- Multi-layer PCB (ground plane)
- Reduce impedance
- Grounding track // and near signal track
- Grounding: grid or ground plane
- SMD (to reduce loop surface, length, PCB size)
- ...

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Circuit design and grounding

Track impedance

200 mV
\[ \text{à } I(f) = 50 \text{ mA} \]

\[ |I_f| \text{ (dBΩ)} \]

\[ |V_f| \text{ (dBmV)} \]

V(f)

\[ I(f) \]

100 mΩ

60 nH

10 cm

\[ \begin{align*}
\text{circuit équivalent d'une} \\
\text{piste de cuivre de} \\
35 \text{ microns,} \\
\text{longueur 10 cm,} \\
\text{largeur 0,5 mm}
\end{align*} \]

\[ \begin{align*}
\text{inductance} \\
\text{approx.} \\
60 \text{ nH}
\end{align*} \]

\[ \begin{align*}
\text{impédance} \\
\text{à 30 MHz} \\
11,3 \Omega
\end{align*} \]

\[ \begin{align*}
30 \text{ nH} & \quad 5,6 \Omega \\
16 \text{ nH} & \quad 3,0 \Omega \\
18 \text{ nH} & \quad 3,4 \Omega \\
\end{align*} \]

\[ \begin{align*}
1 \text{ cm} \\
2 \text{ mm}
\end{align*} \]

\[ \begin{align*}
0,5 \text{ mm}
\end{align*} \]
Grid or meshed grounding

The number of return path for current to ground should be important to reduce $L$. Tracks with width $\gg$

The comb configuration is not a good solution.
S détermine dans tous les cas l’inductance globale de la boucle

pistes parallèles

pistes de part et d’autre de la platine

plan de masse sur la face opposée de la platine, offre un chemin de retour à toute piste de l’autre côté

5.13
- Do not interrupt ground plane
- If this interruption is mandatory, add a bridge (as short as possible and near the critical track)
- No slot in the ground plane (multi-layer is ideal).
Design rules
For electronic circuits and PCBs (part II)

Véronique Beauvois, Ir.
2019-2020
Harm. impaires

Harm. paires et impaires
How to choose the logic family?
Radiated emission of circuits

Differential mode
R.E.

Common mode
R.E.

Table 6.1

Table 6.2
Loop = small if dimensions < λ/4, means 1m @ 75MHz
IC loops could be considered as small up to some 100 MHz
Maximum E-field of this loop @ 10 m measurement distance:
E (V/m) = 263 x 10^{-12} x f(MHz)^2 x A(cm^2) x I_S (mA)  --->  +40dB/dec
According to:
\[ E \text{ (V/m)} = 263 \times 10^{-12} \times f(\text{MHz})^2 \times A(\text{cm}^2) \times I_s (\text{mA}) \quad \text{---} \quad 40 \text{ dB/dec} \]

Question: this PCB needs or not an additional shielding?
A=10 cm\(^2\) ; I_s=20 mA and f=50 MHz
E=42 dB\(\mu\)V/m means 12dB over the limit in class B
So if current I and frequency f are fixed, A could not be reduced, a shielding is necessary.
<table>
<thead>
<tr>
<th>Famille logique</th>
<th>$t_1/t_2$</th>
<th>$\Delta t$</th>
<th>Surface de boucle en cm$^2$ : fréquence d’horloge</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ns</td>
<td>mA</td>
<td>4 MHz</td>
</tr>
<tr>
<td>4000B CMOS à 5 V</td>
<td>40</td>
<td>6</td>
<td>1000</td>
</tr>
<tr>
<td>74HC</td>
<td>6</td>
<td>20</td>
<td>45</td>
</tr>
<tr>
<td>74LS</td>
<td>6</td>
<td>50</td>
<td>18</td>
</tr>
<tr>
<td>74ALS</td>
<td>3,5</td>
<td>50</td>
<td>10</td>
</tr>
<tr>
<td>74AC</td>
<td>3</td>
<td>80</td>
<td>5,5</td>
</tr>
<tr>
<td>74F</td>
<td>3</td>
<td>80</td>
<td>5,5</td>
</tr>
<tr>
<td>74AS</td>
<td>1,4</td>
<td>120</td>
<td>2</td>
</tr>
</tbody>
</table>

Surface de boucle pour 30 dBµV/m 30 MHz - 230 MHz, 37 dBµV/m 230 MHz - 1000 MHz à 10 m

Utilisation : prenons l’exemple de la famille 74ALS avec $F_{\text{clk}} = 30$ MHz.
Le cas le plus défavorable est à 150 MHz (5$\text{ème}$ harmonique)

L’analyse de Fourier de la source de courant, en utilisant la section C.7 avec $(t_1 + t_2) / T = 0,5$ ; $T = 33,3$ ns ; $t_1 = 3,5$ ns et $I = 50$ mA, donne 3,83 mA pour $I_{(5)}$
le courant du cinquième harmonique.

De l’équation (4.6), pour un champ $E$ de 30 dBµV/m et $I_{(5)}$ comme ci-dessus à 150 MHz, la surface de boucle admissible est de 1,395 cm$^2$ (arrondi à 1,4 dans le tableau).

Tableau 6.1 – Émission en mode différentiel : surface maximale permise.

≈ Dim. case

Shielding + filtering

dynamic commutation current / component to charge or discharge the capacitor

Limit EN 55022 cl.B
C.M. ----> R.E. of PCB

Cable length resonance @ 30-100MHz

\[ E \text{ (V/m)} = 1.26 \times 10^{-4} \times f(\text{MHz}) \times L(\text{m}) \times I_{MC} (\text{mA}) \]

if the cable is represented by a short monopole (\(L<\lambda/4\)) @ 10m of the ground e.g. 1m of cabling, \(E = 42\text{dB} \mu \text{V/m}\), then \(I_s = 20\mu \text{A} (/1000#I_{MD})\)
CM voltage to cable, \( \Delta I \) on ground path
Differential noise voltage \( V_N = \Delta I j\omega L \)
(between reference ground and cable connection)
\( Z \approx 150\Omega \) (constant with f)
### Émissions en mode commun : longueur de piste admissible

<table>
<thead>
<tr>
<th>Famille logique</th>
<th>$t_s/t_f$</th>
<th>$\Delta f$</th>
<th>Longueur de plate en cm : fréquence d’horloge</th>
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Longueur de piste autorisée pour 30 dB$\mu$V/m 30 MHz - 230 MHz, 37 dB$\mu$V/m 230 MHz - 1000 MHz à 10 m :

- longueur du câble = 1 m ; agencement : pistes parallèles de 0,5 mm distantes de 0,5 mm (2,8 nH/cm).

Utilisation : prenons par exemple la famille 74HC avec $F_{cl} = 10$ MHz. Le cas le plus défavorable est à 90 MHz (9ème harmonique).

À partir de l’équation (4.7), pour une intensité de champ $E$ de 30 dB$\mu$V/m et 1 m de câble, $I_{CM}$ doit être égal à 2,8 $\mu$A.

Selon $V_N = I_{CM} \times 150$, avec l’atténuation de couplage de 20 dB, $V_N = 4,18$ mV.

L’analyse de Fourier de la source de courant, en utilisant la section C.7 avec $(t + t_f)/T = 0,5$ :

- $T = 100$ ns ; $t_f = 6$ ns et $I = 20$ mA, donne 0,826 mA pour $I_{(9)}$, le courant du neuvième harmonique.

Ensuite, suivant $I = V_N/2\pi f(9)$, l’inductance aux bornes de laquelle on peut admettre $V_N$ à $I_{(9)}$ et 90 MHz est de 8,95 nH, soit 3,19 cm autorisés à 2,8 nH/cm.

### Tableau 6.2 – Émissions en mode commun : longueur de piste admissible.
R.E. - Comparaison CM / DM

For the same signal in DM or CM
trapezoidal @ 12MHz, with \( t_r \) and \( t_f \) 3.5ns
CM Ipk 0.1mA in cable, with L 2m
DM 20mA in a loop of 5cm²

\[
E (V/m) = 263 \times 10^{-12} \times f(MHz)^2 \times A(cm^2) \times I_S (mA) \quad \text{loop-IC}
\]

\[
E (V/m) = 1.26 \times 10^{-4} \times f(MHz) \times L(m) \times I_{MC} (mA) \quad \text{antenna-cable}
\]
R.E. > main source processor clock

Commercial standards: no difference between N.B. and B.B.
- To reduce N.B. with buffer on lines and take care of ground plane.
- To reduce B.B. sources on data lines, video...