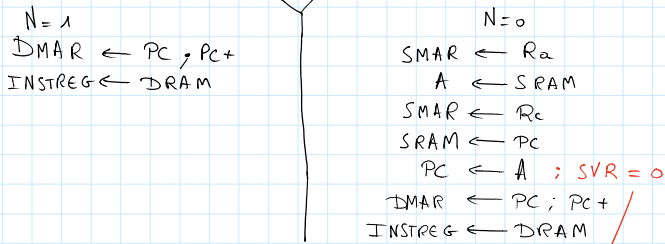


1) Jump and branch instructions and SVR control signal.

→ MSB implemented explicitly: ALWAYS have to specify SVR = 0 or 1 when storing something in PC (see slide PC)

JMPB (Ra, Rb, Rc) - User

SMAR ← Rb
B ← SRAM
B ← B ; Latch



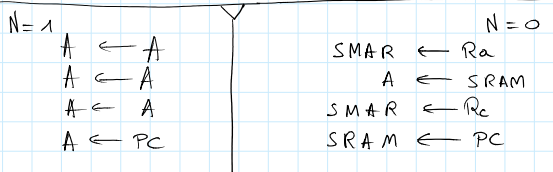
We can never jump to a privileged address from user mode.

Besides, PC31 is implemented explicitly → need to tell its value when modifying PC!

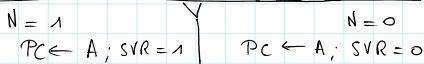
2) Branch has a subbranch? No problem (see slide instreg)

JMPB (Ra, Rb, Rc) - SVR

SMAR ← Rb
B ← SRAM
B ← B ; Latch



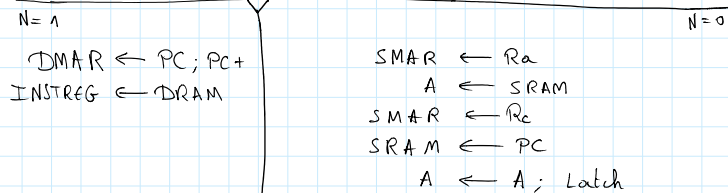
A ← A ; Latch



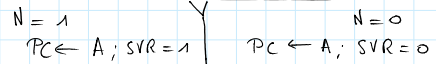
DMAR ← PC ; PC+
INSTREG ← DRAM

JMPB (Ra, Rb, Rc) - SVR mode

SMAR ← Rb
B ← SRAM
B ← B ; Latch

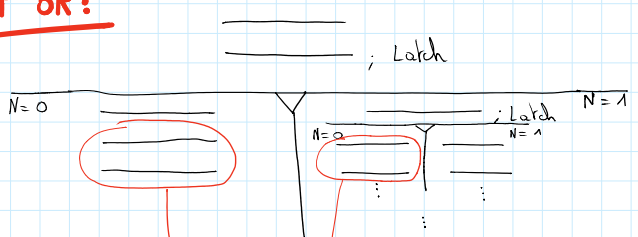


A ← A ; Latch



DMAR ← PC ; PC+
INSTREG ← DRAM

NOT OK:



Same phase, same flag value
Latched

→ Same phase, same flag value
↳ Same inputs for control ROM!
⇒ Code covering: BAD