TP 3 corrections

vendredi 2 octobre 2015 15:24

1) Jump and branch instructions and SVR control signal.

→ MSB implemented (explicitely) : ALWAYS have to specify SVR = 0 or 1 when storing something in PC (see slide PC)

JMPB (Ra, Rb, Rc) — User

SMAR ← Rb
B ← SRAM
B ← B ; Latch

N = 1
DMAR ← PC ; PC+
INSTREG ← DRAM

N = 0
SMAR ← Ra
A ← SRAM
SMAR ← Rc
SRAM ← PC
PC ← A ; SVR = 0
DMAR ← PC ; PC+
INSTREG ← DRAM

We can never jump to a privileged address from user mode.

Besides, PC 31 is implemented explicitly → need to tell its value when modifying PC!

2) Branch has a subbranch ? No problem (see slide imstreg)

JMPB (Ra, Rb, Rc) — SVR

SMAR ← Rb
B ← SRAM
B ← B ; Latch

N = 1
A ← A
A ← A
A ← A
A ← PC

N = 0
SMAR ← Ra
A ← SRAM
SMAR ← Rc
SRAM ← PC

A ← A ; Latch

N = 1
PC ← A ; SVR = 1

N = 0
PC ← A ; SVR = 0

DMAR ← PC ; PC+
INSTREG ← DRAM

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JMPB (Ra, Rb, Rc) — SVR mode

SMAR ← Rb
B ← SRAM
B ← B ; Latch

N = 1
DMAR ← PC ; PC+
INSTREG ← DRAM

N = 0
SMAR ← Ra
A ← SRAM
SMAR ← Rc
SRAM ← PC
A ← A ; Latch

N = 1
PC ← A ; SVR = 1

N = 0
PC ← A ; SVR = 0

DMAR ← PC ; PC+
INSTREG ← DRAM

NOT OK :

; Latch

N = 0 N = 1

; Latch

N = 0 N = 1

Phase
0
1
2
3
4
⋮

Same phase, same flag value

Same phase, same flag value

↳ Same inputs for control ROM !

⇒ Code covering : BAD