Embedded Systems
Examination session of January 2021

Notes or documents of any kind forbidden. Duration: 2 h 30.

Each question must be answered on a different sheet with your name and section.

1. A light intensity sensor connected to an I^2C bus has the fixed address 0x11. When it is addressed, it immediately replies with 8 bits of information representing the incident light level.

   (a) A microcontroller starts an I^2C transaction for reading the current light level from the sensor. Assuming that the received value is equal to 0x21, describe bit by bit the data exchanged over the bus during this transaction, by providing the value of each bit and the direction in which it is transmitted. (Justify all the elements of your answer.)

   (b) The software running on this microcontroller is composed of the following tasks:
   - A task reading the current light level from the sensor every 100 ms. This task relies on an integrated I^2C module of the microcontroller, that is able to begin and finish transactions, and to send and receive bytes of data. This module sends an interrupt request when a transmitted byte of data (including the first one) has been acknowledged by a slave (either positively or negatively), as well as when a byte of data has been received from a slave.
   - A task computing every 10 ms a value derived from the current and past measured light levels, and updating a display accordingly. The computation time of this task is less than 2 ms.

   What is the most appropriate software architecture for this software? (Justify your answer.)

   (c) In pseudocode, give the global structure of this software, with enough details to show data communication between tasks, with interrupt routines, and with the I^2C peripheral.

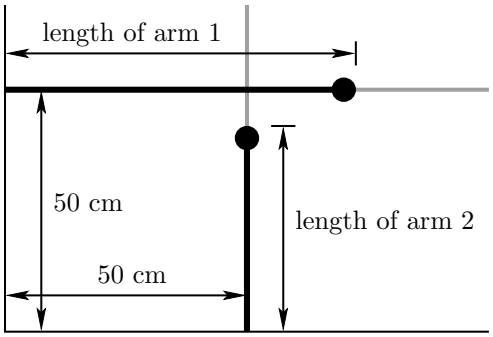
2. Consider two periodic tasks τ_1 and τ_2, with respective priorities P_1, P_2, periods T_1, T_2, and execution times C_1, C_2, such that $P_1 > P_2$ and $T_1 < T_2$.

   Assuming that these tasks fully use the processor, and that they both start their execution at $t = 0$, it is known that one has

$$C_2 = \begin{cases} T_2 - C_1 \left\lceil \dfrac{T_2}{T_1} \right\rceil & \text{if } \tau_1 \text{ is inactive at } t = T_2, \\ (T_1 - C_1) \left\lfloor \dfrac{T_2}{T_1} \right\rfloor & \text{otherwise.} \end{cases}$$

   Under those assumptions, what is the value of C_1 (expressed in terms of T_1 and T_2) that leads to the smallest possible value of the processor load factor? (Carefully explain all the steps of your reasoning.)

3. An industrial pick-and-place robot is composed of two telescopic arms that extend and retract along two orthogonal rails, as illustrated below (the rails are depicted in gray):



The arms cannot cross each other: If any of them is extended by more than 50 cm, then the length of the other one must be less than 50 cm, otherwise a collision occurs.

Both arms move independently, in the following way. Initially, they are fully retracted (meaning that their length is 0 cm). Then, after a delay between 10 and 100 ms, they extend at the constant speed of 1 m/s. After reaching a length of 1 m, they wait between 10 and 100 ms, before fully retracting (also at the speed of 1 m/s). This procedure is then repeated again and again. Whenever a collision occurs, the arm with the shortest length (or both if they are extended by exactly the same amount) immediately starts to retract. After being fully retracted, it then carries out the next actions in its cycle: waiting, extending, waiting, retracting, and so on.

Model the behavior of this device with a hybrid system, with one process for each arm, and a dedicated variable counting the total number of arm retractions that result from collisions.