Embedded Systems
Examination session of January 2019

Notes or documents of any kind forbidden. Duration: 3 h 30.

Each question must be answered on a different sheet with your name and section.

1. (a) What are the advantages of connecting the internal components of an embedded system to a bus (with respect to other types of communication channels)? Give three mechanisms that must be implemented by such a bus, and explain their purpose. [2/20]

   (b) Describe the sequence of operations performed by a processor when it receives an interrupt request. [1/20]

   (c) Explain how different tasks of a real-time operating system can communicate together. [1/20]

   (d) Two periodic tasks τ_1, τ_2 are characterized by their respective periods $T_1 = 1$ ms and $T_2 = 3.5$ ms. The execution time C_1 of τ_1 is equal to 0.6 ms. For which value(s) of C_2 does this pair of tasks fully use the processor? (Justify all steps of your reasoning.) [2/20]

2. A bicycle speedometer works by computing the speed of the bike based on the time required by its wheels to make a complete rotation. For this, the bike is equipped with a magnet attached to its front wheel, and with a magnetic sensor attached to its frame at the same level as the magnet.

   The speedometer includes a microcontroller that periodically samples the output of the magnetic sensor. The value of this sensor reaches a peak whenever the magnet passes in front of the sensor, indicating that the wheel just made a complete rotation. When that happens, the microcontroller starts computing the current speed of the bike. The sensor is sampled every 100 μs, and this operation takes a negligible amount of time. Computing the speed requires 30 μs.

   In addition to computing and displaying the speed of the bike, the speedometer offers additional features such as memorizing statistics (total distance traveled, average and maximum speed, ...) in flash memory, and displaying them on demand when a button is pressed.

   - Computing statistics and writing them into flash memory is done every second, and requires 10 μs. However, the flash memory component requires 15 ms of additional time to complete the write operation. It triggers an interrupt upon completion of this operation.
   - The display should be refreshed every 20 ms, and this operation needs 15 μs of processor time.
   - The state of the button is sampled at the same time as the sensor, and requires negligible time.

(a) What is the best software architecture for this system? Justify carefully your answer. [3/20]

(b) Using pseudocode, give the global structure of this software. [3/20]

3. A production line in a snack factory contains a machine that outputs chocolate bars side by side, on a conveyor belt moving at the speed of 1 m/s. The bars have a width of 2 cm and are produced every 0.1 s to 0.15 s.

   In order to assemble chocolate bars in packs of two, a pairing device is added to this conveyor belt. It consists in a sensor detecting passing bars, and a gate that can block them. The idea is to close the gate long enough that two bars are blocked, and then to open it so as to release the newly formed pair of bars on the conveyor belt. The cycle then repeats with the next two bars. This device is designed as follows:

   - A sensor located 8 cm upstream of the gate is able to detect passing bars, and triggers the opening of the gate every two detections.
   - When the gate is opened, it remains in that state for 60 ms, and closes automatically after this delay.
   - The gate is assumed to open and close in negligible time.

   (a) Model the behavior of the pairing device with a hybrid system. The conveyor belt can be assumed to be initially empty. [5/20]

   (b) Explain how to check, with the help of the model obtained at the previous step, whether there exists a risk of crushing a bar in the gate, or letting a single bar or a group of more than two bars pass the gate (with the current parameters of the system). Illustrate your answer by carrying out in detail the first three steps of the procedure. [3/20]