

# ELEN0037

## Microelectronics

### Tutorials

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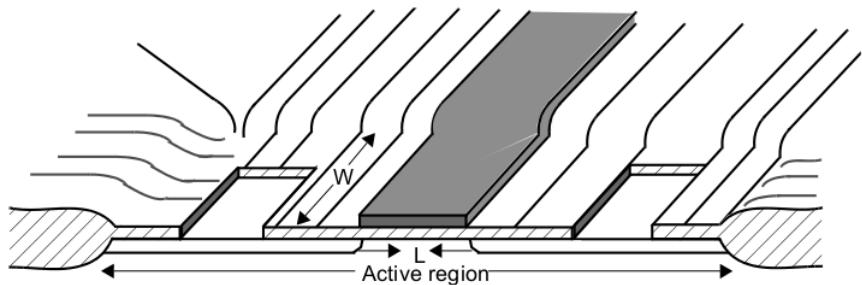
With special thanks to Vincent Pierlot

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Tutorial 2: Technological Aspects and Components

## Layout design rules (1)

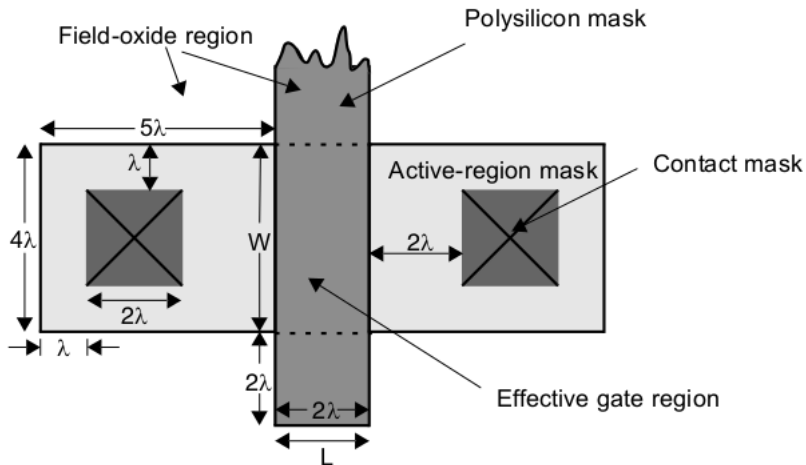
Simplified view of a partially finished MOS transistor and its important dimensions:



- The design rules are expressed in terms of  $\lambda$ .
- Minimum gate length:  $L_{min} = 2\lambda$ .

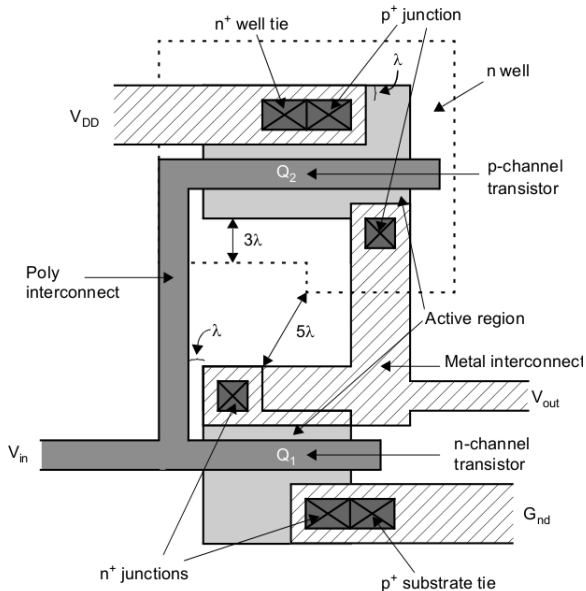
## Layout design rules (2)

The corresponding layout of the active, polysilicon, and contact masks of the smallest transistor that can be realized in a given process when a contact must be made to each junction:



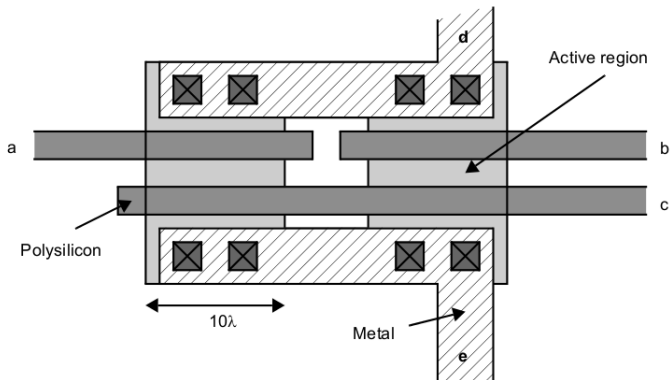
## Layout design rules (3)

A possible layout of a CMOS inverter with several design rules:



## Exercise 1 (1st/2nd, P2.9)

Find the circuit that the layout shown hereunder realizes. Simplify the circuit, if possible,<sup>1</sup> and give the sizes of all transistors.<sup>2</sup> Assume  $L = 2\lambda$ , where  $\lambda = 1\mu m$ .

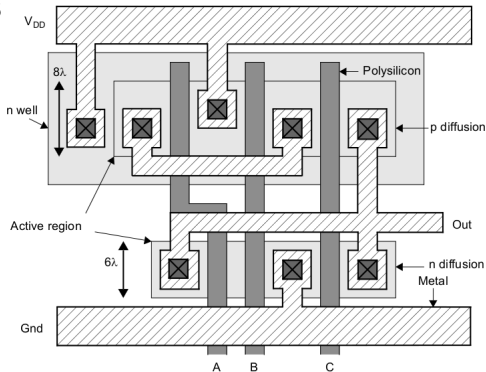


<sup>1</sup>in the case of a digital circuit, it could be the “pull-down” part of the function:  $d = c \cdot (a + b)$ , if  $e$  is connected to ground

<sup>2</sup>size of the transistors:  $10/2$

## Exercise 2 (1st/2nd, P2.10)

Find the schematic for the CMOS logic circuit realized by the layout shown hereunder.<sup>3</sup> Give the widths of all transistors.<sup>4</sup> Assume  $L = 2\lambda$ , where  $\lambda = 0.4\ \mu\text{m}$ . In tabular form, give the area and perimeter of each junction.<sup>5</sup>



$$^3 \text{out} = \overline{ab + c} = (\overline{a} + \overline{b}) \overline{c}$$

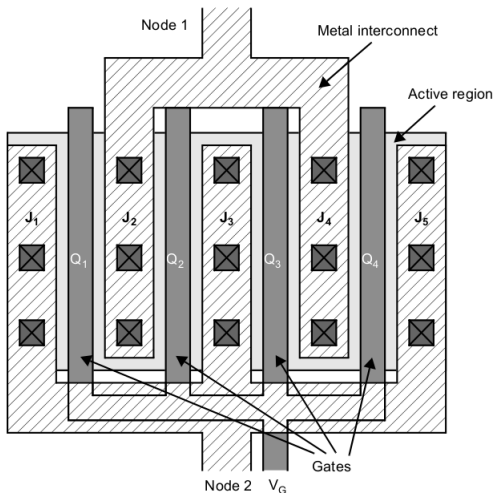
<sup>4</sup> top  $\rightarrow$  down, left  $\rightarrow$  right: 3.2/0.8, 3.2/0.8, 3.2/0.8, 2.4/0.8, 2.4/0.8, 2.4/0.8

<sup>5</sup> area ( $\mu\text{m}^2$ ): 7.68, 7.68, 7.68, 7.68, 5.76, 1.92, 5.76, 5.76

<sup>6</sup> perimeter ( $\mu\text{m}$ ): 8, 4.8, 4.8, 8, 7.2, 1.6, 4.8, 7.2

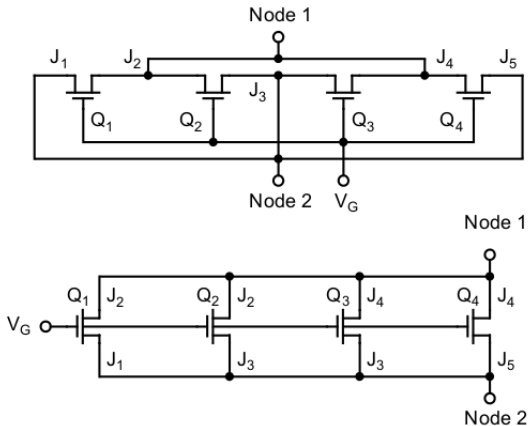
## Exercise 3 (1st/2nd, E2.2, P2.12, P2.13)

Consider the transistor shown in the layout hereunder, where the total width of the four parallel transistor is  $80\lambda$ , its length is  $2\lambda$ , where  $\lambda = 0.5\ \mu\text{m}$ .



## Exercise 3 (cont)

The schematic drawn in the same relative positions as the layout, and the circuit redrawn to make the parallel transistors more obvious are:



Assume node 1 is the drain, node 2 is the source, and the device is in the active region.



## Exercise 3 (cont)

- 1 Find the source-bulk and the drain-bulk capacitances. Assume  $C_j = 2.4 \times 10^{-4} \text{ pF}/(\mu\text{m})^2$ , and  $C_{j-sw} = 2.0 \times 10^{-4} \text{ pF}/\mu\text{m}$ .<sup>7</sup>
- 2 Find the equivalent capacitances if the transistor were realized as a single device with source and drain contacts still evenly placed.<sup>8</sup>
- 3 Repeat the same exercise, where an overall transistor width of  $80\lambda$  is still desired, but with 8 parallel transistors of width  $10\lambda$ .<sup>9</sup>
- 4 Repeat the same exercise, where an overall transistor width of  $80\lambda$  is still desired, but with 2 parallel transistors of width  $40\lambda$ .<sup>10</sup>

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<sup>7</sup>  $C_{sb} = 0.036 \text{ pF}$ ,  $C_{db} = 0.017 \text{ pF}$

<sup>8</sup>  $C_{sb} = 0.043 \text{ pF}$ ,  $C_{db} = 0.033 \text{ pF}$

<sup>9</sup>  $C_{sb} = 0.034 \text{ pF}$ ,  $C_{db} = 0.019 \text{ pF}$

<sup>10</sup>  $C_{sb} = 0.044 \text{ pF}$ ,  $C_{db} = 0.016 \text{ pF}$

## Exercise 4 (1st, P2.14, P2.15, 2nd, P2.20)

We desire to match two capacitors of relative sizes 9 and 4.523.

- 1 Draw a layout for the two capacitors such that their ratio will be maintained during overetching.<sup>11</sup>
- 2 Given that a unit-sized capacitor is  $5\ \mu\text{m} \times 5\ \mu\text{m}$  and that the e-beam lithography rounds all sizes to  $0.1\ \mu\text{m}$ , what is the matching accuracy due to rounding of the capacitors?<sup>12</sup>
- 3 What is the new matching accuracy if the capacitor sizes are doubled to 18 and 9.046?<sup>13</sup>

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<sup>11</sup>  $C_1 = 9$  squares,  $C_2 = 3$  squares plus a rectangle with ratio  $0.631 \times 2.415$

<sup>12</sup> matching acc. = 1.9785 (theoretical matching acc. = 1.9898),  $\Rightarrow -0.6\%$

<sup>13</sup> matching acc. = 1.9927 (theoretical matching acc. = 1.9898),  $\Rightarrow +0.15\%$

## Exercise 5 (1st, P2.16, P2.17)

- Given that a polysilicon layer has  $7 \Omega/\square$ , what is the resistance of a long line that is  $2 \mu\text{m}$  wide and  $1000 \mu\text{m}$  long?<sup>14</sup> (Ignore any contact resistance)
- Now assume that the previous resistive line is laid out in a serpentine manner, where enough bends are used such that a line drawn along the middle of the serpentine resistor has a length  $1000 \mu\text{m}$ . Assume the fingers have length  $10 \square$  (the last finger length might be shorter). The bend width is  $3 \square$ , but contributes for  $2.11 \square$ . The contact area is  $1 \square$ , but contributes for  $0.14 \square$ . Compute the resistance of the serpentine, as well as the resulting height and width of the overall layout.<sup>15</sup> How should we modify the serpentine in order to approach the desired resistance?<sup>16</sup>

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<sup>14</sup>  $R = 3.5 \text{ k}\Omega$

<sup>15</sup>  $R = (10 \times 38 + 2.11 \times 38 + 6 + 2 \times 0.14) \times 7 = 3265 \Omega$  ( $24 \mu\text{m} \times 154 \mu\text{m}$ )

<sup>16</sup> 41 “fingers” and “bends”, and 3 single squares, plus the two contacts

## Exercise 6 (2nd, E1.19, E1.21)

- In many CMOS manufacturing processes, polysilicon strips are used to provide a controllable sheet resistance for analog design. A typical value is  $R_{\square} = 500 \Omega$ . If each strip is  $1 \mu\text{m}$  wide and  $5 \mu\text{m}$  long, how many must be connected in series to make a resistor of value  $50 \text{ k}\Omega$ ?<sup>17</sup>
- As before, you require a resistor of value  $50 \text{ k}\Omega$ . However, since the voltage across the resistor is never expected to exceed  $200 \text{ mV}$ , you decide it is feasible to use a NMOS in triode to implement it. You elect to use multiple NMOS sized  $W/L = 2 \mu\text{m}/1 \mu\text{m}$  to avoid short-channel effects. If  $\mu_n C_{ox} = 300 \mu\text{A}/\text{V}^2$ ,  $V_{tn} = 0.3 \text{ V}$ , and you elect to use  $V_{GS} = 1 \text{ V}$ , find the number of series NMOS required to implement the resistor.<sup>18</sup> Compare the resulting total area to that calculated in the first part for a strip resistor.<sup>19</sup>

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<sup>17</sup>  $n = 20$

<sup>18</sup>  $n = 21$

<sup>19</sup>  $A_{strip} = 20 \times (1 \times 5 \mu\text{m}^2)$ ,  $A_{mos} = 21 \times (1 \times 2 \mu\text{m}^2)$