System on a Chip

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Lecture 3: Sample and Hold Circuits
Switched Capacitor Circuits

- Circuits and Systems
  - Sampling
  - Signal Processing
  - Sample and Hold

- Analogue Circuits
  - Switched Capacitor Circuits
Signal Characterisation

- Value and timing can be continuous or discrete

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Time-continuous Signals

- **Continuous or analogue signal**
  - The signal is continuous in value (amplitude) and time
  - The signal is a continuous function of time
  - Examples: voltage, $v(t)$, sound pressure $p(t)$

- **Digitized signal**
  - The signal is discrete in value but not in time
  - Change of value can occur at any instance in time
Time-discrete Signals

- Time discrete signals: function values between sampling points do not exit
  - They are not zero
  - Time discrete signals usually are created by sampling of analogue signals $A(t) \rightarrow a(nT)$
    - $T$: sampling time, $1/T$: sampling rate, sampling frequency

- Discrete time signal: signal is continuous in amplitude and time-discrete
  - Usually sampling occurs at a fixed time interval
  - Or the sample times are known (otherwise loss of information)
  - Nyquist theorem: sampling frequency larger than twice the highest analogue frequency content
    - No information loss
Digital signals are discrete in value (amplitude) and time-discrete

- Usually (but not always) a fixed clock frequency is assumed
- Amplitude discretization means information loss
- n-bit binary signal with $2^N$ possible values
Signal Characterisation

- Value and timing can be time-continuous or discrete

**Continuous values**

**Discrete values**
Time-discrete Signals

- A signal is a mathematical function of the independent variable \( t \)
- For \( t \) continuous, the signal is time-continuous: analogue signal
- If \( t \) is only defined for discrete values, we have a time-discrete signal or sequence \( x[n] \)
- Typically, the sequence \( x[n] \) is created by a discretisation of time by (ideal) sampling at the interval \( T_s \).
- \( x[n] = x(t=nT_s) \)
- Examples:

\[
\delta[n] = \delta[n,0] = \begin{cases} 
1 & \text{for } n = 0 \\
0 & \text{for } n \neq 0 
\end{cases}
\]

Shifted discrete Dirac impulse

\[
\delta[n-i] = \delta[n,i] = \begin{cases} 
1 & \text{for } n = i \\
0 & \text{for } n \neq i 
\end{cases}
\]
### Elementary Time-discrete Signals

- **Unit step sequence**
  
  \[ u[n] = \begin{cases} 
  0 & \text{for } n < 0 \\
  1 & \text{for } n \geq 0 
  \end{cases} \]

- **Sampled Sine/Cosine signal**
  
  \[ x[n] = \cos(2\pi f_0 n T_S) = \cos(\Omega n) \]
  
  - With normalized sampling frequency:
    \[ \Omega = 2\pi f_0 T_S = 2\pi f_0 / f_S \]

- **Rectangular impulse with width 2N+1**
  
  \[ \text{rect}_N[n] = \begin{cases} 
  1 & \text{for } |n| \leq N \\
  0 & \text{otherwise} 
  \end{cases} \]
Any time discrete sequence can be represented by time-shifted unit pulses:

\[ x[n] = \sum_{i=-\infty}^{\infty} x[i] \delta[n-i] \]

**Example**

\[ x[n] = 0\delta[n] + x[1]\delta[n-1] + x[2]\delta[n-2] \]
A time discrete signal is periodic with a period \( N \) if:

\[
x_p[n] = x_p[n + N]
\]

- **\( \text{N: Period} \)**: smallest positive \( N \) that fulfills above equation: fundamental period.
- **Note**: The discrete sine function \( x[n] = \sin(2\pi f_0 n T_s) \) is in general not periodic.
  - It is only periodic of the ratio \( T_0 / T_s = f_s / f_0 \) is an integer.
Definition Signal to Noise Ratio

\[ \text{SNR}_{\text{Digital}} = 10 \log_2 2^N \]

\[ \text{SNR}_{\text{Analog}} = 10 \log_2 \frac{V_{\text{max, eff}}^2}{V_n^2} \]
## Enhancing Analog Dynamic Range

### Solution:
- Chip cooling
- Increase power supply voltage
- Noise reduction using averaging /circuit tricks
- Increasing of components area

### Potential problems:
- Equipment cost & volume problems
- Voltage breakdown; power consumption
- Moderate increase of chip area & speed reduction
- Drastic increase of chip area
## Comparison Analog/Digital Dynamic Range

<table>
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<tr>
<th>Analog design</th>
<th>Digital design</th>
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<td>Signals have a range of values for amplitude and time</td>
<td>Signal have only two states</td>
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<tr>
<td>Irregular blocks</td>
<td>Regular blocks</td>
</tr>
<tr>
<td>Customized</td>
<td>Standardized</td>
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<tr>
<td>Components have a range of values</td>
<td>Components with fixed values</td>
</tr>
<tr>
<td>Requires precise modelling</td>
<td>Modelling can be simplified</td>
</tr>
<tr>
<td>Difficult to use with CAD</td>
<td>Amenable to CAD methodology</td>
</tr>
<tr>
<td>Designed at the circuit level</td>
<td>Designed at the system level</td>
</tr>
<tr>
<td>Longer design times</td>
<td>Short design times</td>
</tr>
<tr>
<td>Two or three tries are necessary for success</td>
<td>Successful circuits the first time</td>
</tr>
<tr>
<td>Difficult to test</td>
<td>Amenable to design for test</td>
</tr>
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</table>
Comparison of Analog and Digital Circuit

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<th></th>
<th>Analog</th>
<th>Analog</th>
<th>Digital</th>
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<tr>
<td>Power supply noise immunity</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Functional density</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
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</table>

- Analog Input (In) and Output (Out) with power supply V_{DD}
- Analog Output (Out) with power supply V_{SS}
- Digital Input (In) and Output (Out) with power supply V_{DD}
Ideal capacitors are noiseless
But capacitors always have to be charged through a resistor
Noise accumulated on a capacitor is independent of the charging resistor
- Noise bandwidth and resistor value cancel out
- For low noise, decrease temperature or increase capacitor

\[ \text{Noise Power Density: } 4 \, kT \]

\[ \text{Eq, Noise Bandwidth: } \frac{1}{4} \frac{1}{RC} = \frac{\pi}{2} f_0 \]

Noise Power: \( kT/C \)
- Ideal capacitors are noiseless
- But capacitors always have to be charged through a resistor
- Noise accumulated on a capacitor is independent of the charging resistor
  - Noise bandwidth and resistor value cancel out

**kT/C Noise RC Circuit**

**SC-Circuit**

![SC-Circuit Diagram]

- Noise Power Density
- Wideband Noise $kT/C$
- Downsampled Noise $kT/C$

![Noise Power Density Graph]

- $V_{IN}$
- $R$
- $C$
- Clock
- $F_{Clock}/2$
- $1/4\;RC$
- $0$
- $V^2_{Noise}$
Sample and Hold Circuits

- S/H is used to sample an analog signal and to store its value for some length of time.
- Also called “track-and-hold” circuits:
  - Often needed in A/D converters.
  - Conversion may require held signal:
    - reduces errors due to different delay times in A/D converter.
- Performance parameter and errors in S/H:
  - **Sampling pedestal** or **Hold Step**:
    - errors in going from track to hold: held voltage is different to sampled input voltage.
    - should be minimized and signal independent for no distortion.
  - **Signal feedthrough**: should be small during hold.
  - **Speed** at which S/H can track input voltage:
    - limitations to bandwidth and slew-rate.
  - **Droop rate**: slow change in output voltage during hold mode.
  - **Aperture (or sampling) jitter**: effective sampling time changing every T
    - difficult in high-speed designs.
- Other errors: dynamic range, linearity, gain, and offset error.
Basic Concept

- If $\phi_{clk}$ is high, $V'$ follows $V_{in}$
- If $\phi_{clk}$ is low, $V'$ will stay constant, keeping the value when went $\phi_{clk}$ low
- Basic circuit has some practical problems: **Charge Injection** of Q1
  - Causes (negative) hold step
- **Aperture Jitter**
  - Sampling time variation as a function of $V_{in}$
When $\phi_{\text{clk}}$ goes low, channel charge on Q1 causes $V'$ to have negative step
  
  - If clock edge is fast, 1/2 flows each way

Channel charge:

\[
\Delta Q_{C_{\text{hld}}} = \frac{Q_{\text{CH}}}{2} = \frac{C_{\text{ox}}WL V_{\text{eff-1}}}{2}
\]

\[
V_{\text{eff-1}} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in}
\]

Resulting in:

\[
\Delta V' = \frac{\Delta Q_{C_{-\text{hld}}}}{C_{\text{hld}}} = -\frac{C_{\text{ox}}WL(V_{DD} - V_{tn} - V_{in})}{2C_{\text{hld}}}
\]
Charge Injection

- ΔV' linearly related to V_{in}: **gain error**
- ΔV' also linearly related to V_{tn}, which is nonlinearly related to V_{in}: **distortion error** (due to Body effect)
  - Often gain error can be tolerated but not distortion
- Additional change in V' due to the overlap capacitances

\[
\Delta V' \approx C_{ox} W L_{ov} (V_{DD} - V_{SS}) / C_{hld}
\]

- Causes DC offset effect
  - Which is signal independent
  - Usually smaller than charge injection component
  - Can be important if Clk signal has power supply noise → can lead to poor power-supply rejection ratio
**S/H Charge Reduction**

- **Transmission gate:** Charge of equally sized p and n transistor cancel out
  - Charge only cancel when $V_{in}$ in middle between $V_{DD}$ and $V_{SS}$
  - Finite slopes of clock edges make turn of times of p and n transistor different and signal dependent

- **Dummy switch:** clocked by inverse Clk
  - Q2 is 1/2 size of Q1 to match charge injection
  - up to 5 times better than without dummy switch (for fast Clk edges)
  - difficult to make clocks fast enough so exactly 1/2 charge is injected
Finite Slopes of Clock Edges

- Ideal sampling time at the negative-going zero-crossing of $\phi_{\text{clk}}$
- Actual sampling at $V_{\text{clk}} = V_{\text{in}} + V_{\text{tn}}$
  - $Q_1$ turns off
- True sampling time depends on value of $V_{\text{in}}$: distortion
When the clock $\phi_{clk}$ is high, the circuit responds similarly to an Opamp in a unity-gain feedback configuration. When goes low, $V_{in}$ at that time is stored on $C_{hld}$, similarly to a simple S/H. DC offset of buffer is divided by the gain of input Opamp.

**Disadvantages:**
- In hold mode, the Opamp is open loop, resulting in its output saturating at one of the power supply voltages.
  - Opamp must have fast slew rate to go from saturation to $Vin$ in next $Clk$ cycle.
- Sample time, charge injection — input signal dependent.
- Speed reduced due to overall feedback.
**Reduced Slew Rate Requirement**

- In Hold mode, Q2 keeps the output of the first Opamp close to the voltage it will need to be at when the S/H goes into track mode.
- Sample time, charge injection - input signal dependent.

![Diagram showing Opamps and clock signals with V_{in} to V_{out} connections]
Input Signal Independence

- $C_{\text{hld}}$ is not to Gnd
- Q1 always at virtual ground; signals on both sides are independent of $V_{\text{in}}$
  - Sample time error, charge injection: independent of $V_{\text{in}}$
  - Charge injection causes ONLY DC offset
- Q2 used to clamp Opamp1 output near ground in hold mode
  - Reduces slew rate requirement snd signal feedthrough
- **Slower** due to two Opamps in feedback
Reduced Offset (Single Ended)

- Charge injected by Q1 matched by Q2 into $C'_{\text{hl}}$
  - If fully differential design, matching occurs naturally leading to lower offset.
Reduced Offset (Differential)

- Gnd is common mode voltage
**Example 1: BiCMOS**

- **Inverting S/H**
  - When in track mode, Q1 is on and Q2 is off, resulting in the S/H acting as an inverting low-pass circuit with $\Omega_{-3dB} = 1/(RC)$
  - When Q1 turns off, $V_{out}$ will remain constant
- **Needs Opamp capable of driving resistive loads**
  - Difficult to implement in CMOS
- **Good high-speed BiCMOS configuration**
- **Q2 minimizes feedthrough**
Example 2

- Opamp in unity gain follower mode during track
- In hold mode input signal is stored across C1, since Q1 is turned off
- Charge injection of transistors cancel
- Clock signals are signal dependent
- Good speed, moderate accuracy
- Hold capacitor is large Miller capacitor
- Can use smaller capacitors and switches — good speed
- If Q2 turned off first, injection of Q1 small due to Miller effect
Example 3

- Miller capacitor: 
  \[ C_{\text{hld-eff}} = (1 + A) \left( \frac{C_1C_2}{C_1 + C_2} \right) \]

- Higher speed amplifier possible as Opamp output voltage swing is small
- Allows small capacitors and switch sizes

Sample Mode

- Sample mode:
  - Opamp is reset
  - C1 and C2 between Vin and V of Opamp

Hold Mode

- Hold mode:
  - Effective hold cap is \( C_{\text{hld-eff}} \)
Example 4

- For lower frequency application
  - Based on switched capacitor circuits

- During $\phi_1$:
  - $C_H$ is connected between the input signal source and the inverting input of the Opamp
  - Inverting input and the output of the opamp are connected together
    - This causes the voltages at both of these nodes to be equal to the input-offset voltage of the Opamp, therefore $C_H$ charged to $V_{in} - V_{off}$

- Accurate since offset cancellation performed
  - During $\phi_1$ $V_{out} = V_{in}$ independent of the Opamp offset voltage

- Slow since Opamp swings from 0 to $V_{in}$ every cycle

- Not really a S/H
  - Output not valid during $\phi_1$
Example 5

- Improved accuracy
- High input impedance
- $\phi_{1a} \rightarrow$ advanced
- Charge injection of Q4 and Q5 cancel (and is signal independent)
- Charge injection of Q1 and Q2: no effect
- Charge injection of Q3: reduced as before

In Hold mode
Switched capacitor (SC) circuits are probably the most popular integrated circuit analogue circuit technique.

- SC operate at discrete time / analogue amplitude.
- For the analysis z-transform is most appropriate.
- Especially popular for filters:
  - Good linearity, accurate frequency response, high dynamic range.
  - Filter coefficients make use of capacitance ratios.
Switched Capacitor Circuits

- **Basic principles**
  - Signal entered and read out as voltages, but processed internally as charges on capacitors.
  - Since CMOS preserves charges well, high SNR and linearity are possible.

- **Significance**
  - Replaces absolute accuracy of R & C (10-30%) with matching accuracy of C (0.05-0.2%)
  - Can realize accurate and tunable large RC time constants
  - Can realize high-order circuits with high dynamic range
  - Allows (medium-) accuracy data conversion without trimming
  - Can realize large mixed-mode systems for telephony, audio, aerospace, consumer etc. applications on a single CMOS chip
  - Tilted the MOS VS. BJT contest decisively.
Opamps

- Ideal Opamps usually assumed
- Important non-idealities
  - dc gain: sets the accuracy of charge transfer hence, transfer-function accuracy
  - unity-gain frequency, phase margin & slew-rate: sets the max clocking frequency.
  - A general rule is that unity-gain frequency should be 5 times (or more) higher than the clock-frequency
  - dc offset: Can create dc offset at output. Circuit techniques to combat this which also reduce 1/f noise.
SC Building Blocks

- **Double Poly Capacitors**
  - Substantial parasitics with large bottom plate capacitance (20% of $C_1$)
  - Sometimes metal-metal capacitors are used but have even larger parasitic capacitances.
SC Building Blocks

Switches
- Mosfet switches are good switches off-resistance near GΩ range
- on-resistance in 100Ω to 5kΩ range (depends on transistor sizing)
- However, have non-linear parasitic capacitances
- When φ high, switch is on
SC Building Blocks

- **Non-overlapping clocks**
  - Non-overlapping clocks — both clocks are never High at same time
  - Needed to ensure charge is not inadvertently lost
  - Integer values occur at end of $\phi_1$ i.e. (n-1), n, (n+1) ...
  - End of $\phi_2$ is 1/2 of integer value, i.e. (n-3/2), (n-1/2), (n+1/2) ...

![Diagram](image-url)
Basic Operating Principle

- **Switched-capacitor resistor equivalent**
  - $C_1$ charged to $V_1$ and then to $V_2$ during each Clk period $T$

  \[ \Delta Q_1 = C_1(V_1 - V_2) \]

  - Average current is given by:

  \[ I_{avg} = \frac{C_1(V_1 - V_2)}{T} \]

\[ \phi_1 \quad \phi_2 \]

\[ V_1 \quad \overline{\overline{C_1}} \quad V_2 \]

\[ \Delta Q = C_1(V_1 - V_2) \text{ every clock period} \]

\[ R_{eq} = \frac{T}{C_1} \]
Basic Operating Principle

- Switched-capacitor resistor equivalent
  - For equivalent resistor can be calculated from:

\[ I_{eq} = \frac{V_1 - V_2}{R_{eq}} \]

- Therefore:

\[ R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \]

- This equivalence is useful when looking at low-frequency portion of a SC-circuit
- For higher frequencies, discrete-time analysis is used.
Example Resistor Equivalence

- What is the equivalent resistance of a 5pF capacitance sampled at a clock frequency of 100kHz?

\[ R_{eq} = \frac{1}{(5 \times 10^{-12})(100 \times 10^3)} = 2M\Omega \]

- large equivalent resistance of 2MΩ can be realized
- Requires only 2 transistors, a clock and a relatively small capacitance
- In a typical CMOS process, such a large resistor would normally require a huge amount of silicon area.
Integrator (Parasitic Sensitive)

- Switched capacitor discrete time integrator
  - Extra switch at the output indicates that the output signal is valid at the end of $\phi_1$
  - Input can change at any point in time – it is sampled at the end of $\phi_1$
  - Simplest circuit design but sensitive to parasitics (not shown)

- Calculate $v_{co}(t)$ at the end $\phi_1$ of as a function of $v_{ci}(t)$ at the end of $\phi_1$
Integrator (Parasitic Sensitive)

- Circuit diagrams for $\phi_1$ high and for $\phi_2$ high

- Charge on $C_2$ is equal to $C_2 v_{co}(nT-T)$ when $\phi_1$ is turning off
- Charge on $C_1$ is equal to $C_1 v_{ci}(nT-T)$ when $\phi_1$ is turning off
- When $\phi_2$ goes high $C_1$ is discharged (due to virtual ground on its top plate)
  - Charge is transferred to $C_2$ adding to the charge present there
  - Positive input voltage will result in a negative voltage across $C_2$ (inverting integrator)
- So, at the end of $\phi_2$:
  $$C_2 v_{co}(nT-T/2) = C_2 v_{co}(nT-T) - C_1 v_{ci}(nT-T)$$
Integrator (Parasitic Sensitive)

- Circuit diagrams for $\phi_1$ high and for $\phi_2$ high

- What is the charge on $C_2$ at the end of $\phi_1$ (as indicated by the additional $\phi_1$ switch at the output)?
  - When $\phi_2$ turns off, the charge on $C_2$ is preserved during the next $\phi_1$ phase (until $\phi_2$ turns on again in the next cycle)
  - Therefore the charge on $C_2$ at time $nT$ at the end of the next $\phi_1$ is equal to that at time $(nT-T/2)$

- Therefore:
  \[ C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) \]
  \[ C_2 v_{co}(nT) = C_2 v_{co}(nT - T) - C_1 v_{ci}(nT - T) \]
Integrator (Parasitic Sensitive)

- Circuit diagrams for $\phi_1$ high and for $\phi_2$ high

- Dividing by $C_2$ and introducing discrete time variables $v_i(n)=v_{ci}(nT)$ and $v_o(n)=v_{co}(nT)$:

$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n-1)$$

- Taking the z-transform: $V_o(Z) = z^{-1}V_o(Z) \quad - \frac{C_1}{C_2} z^{-1}V_1(Z)$

- Integrator Transfer Function:

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right) \frac{1}{z-1}$$
Integrator (Parasitic Sensitive)

- Circuit diagrams for $\phi_1$ high and for $\phi_2$ high

- Integrator Transfer Function:

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right) \frac{1}{z - 1}$$

- Gain depends only on capacitor ratios!
  - Very accurate transfer functions can be realised!
- Transfer function is only valid at the time $nT$ just before the end of $\phi_1$
  - Discrete time relationship of $v_{oi}(t)$ and $v_{co}(t)$ is valid only at times $(nT)$ – at the end of $\phi_1$
Low Frequency Behaviour

- The transfer function can be rewritten as:
  \[ H(z) = -\left(\frac{C_1}{C_2}\right)\frac{z^{-1/2}}{z^{-1/2} - z^{1/2}} \]

- Recall that:
  \[ z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T) \]

- With \( T = \frac{1}{f_s} \) →
  \[ z^{1/2} = \cos\left(\frac{\omega T}{2}\right) + j\sin\left(\frac{\omega T}{2}\right) \]

  \[ z^{-1/2} = \cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right) \]

- Therefore:
  \[ H(e^{j\omega T}) = -\left(\frac{C_1}{C_2}\right)\frac{\cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right)}{j2\sin\left(\frac{\omega T}{2}\right)} \]

- For \( \omega T \ll 1 \) (i.e. at low frequency)
  \[ H(e^{j\omega T}) \approx -\left(\frac{C_1}{C_2}\right)\frac{1}{j\omega T} \]
Low Frequency Behaviour

- For $\omega T << 1$ (i.e. at low frequency)
  \[ H(e^{j\omega T}) \approx -\left(\frac{C_1}{C_2}\right) \frac{1}{j\omega T} \]

- This is the same transfer function as a continuous-time integrator with a gain constant of:
  \[ K_I \equiv \frac{C_1}{C_2 T} \]

- The gain is a function of the capacitor ratio and the sampling time
Parasitic Effects

- Assuming double poly capacitors, the circuit diagram with parasitic capacitances is:

- The transfer function modifies to:

  \[ H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right) \frac{1}{z - 1} \]

- Therefore, gain coefficient is not well controlled and partially non-linear, as \( C_{p1} \) is non-linear

\( C_{p1} \): parasitic capacitances of \( C_1 \), top plate and nonlinear capacitances of the two switches

\( C_{p2} \): parasitic capacitances of \( C_1 \), bottom plate

\( C_{p3} \): parasitic capacitances of \( C_2 \), top plate and input capacitances of Opamp and of \( \phi_2 \) switch

\( C_{p3} \): parasitic capacitances of \( C_2 \), bottom plate (and output capacitance)
Parasitic Insensitive Integrator

- By using 2 extra switches, integrator can be made insensitive to parasitic capacitances
  - more accurate transfer-functions
  - better linearity (since non-linear capacitances unimportant)
- Major development for SC circuits
Parasitic Insensitive Integrator

- Circuit diagrams for $\phi_1$ high and for $\phi_2$ high

- Same analysis as before except that $C_1$ is switched in polarity before discharging into $C_2$
  - This results in $v_{co}(t)$ rising for a positive $v_{ci}(nT-T)$

- Therefore:

  $$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right) \frac{1}{z-1}$$

- Non-inverting amplifier!

- But full time period delay as $H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1-z^{-1}}$
Parasitic Insensitive Integrator

- Circuit diagram with parasitic capacitances
  - $C_{p3}$ has little effect since it is connected to virtual Ground
  - $C_{p4}$ has little effect since it is driven by output
  - $C_{p2}$ has little effect since it is either connected to virtual Ground or physical Ground
Parasitic Insensitive Integrator

- $C_{p1}$ is continuously being charged to $v_i(n)$ and discharged to ground
- $\phi_1$ high: the fact that $C_{p1}$ is also charged to $v_i(n-1)$ does not affect charge on $C_1$
- $\phi_2$ high: $C_{p1}$ discharges through $\phi_2$ switch attached to its node and does not affect the charge accumulating on $C_2$
- While the parasitic capacitances may slow down settling time behaviour, they do not affect the discrete time difference equation
Parasitic Insensitive Inverting Integrator

- Present output depends on present input (delay-free)
  \[ H(z) = \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1} \quad \text{or} \quad H(z) = -\frac{C_1}{C_2} \frac{1}{1-z^{-1}} \]

- Delay-free integrator has negative gain while delaying integrator has positive gain

- Delay free, parasitic insensitive inverting integrator:
  - Same circuit, but switch phases at \( C_1 \), top plate, are swapped

\[
C_2 v_{co}(nT - T/2) = C_2 v_{co}(nT - T) \\
C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) - C_1 v_{ci}(nT)
\]
Signal Flow Graph Analysis

- For more complex circuits charge analysis can be tedious
Signal Flow Graph Analysis

- Superposition is used on the input-output relationship for $V_2(z)$ and $V_3(z)$ are given by:

  $$\frac{V_o(z)}{V_2(z)} = \frac{C_2}{C_A} \frac{z^{-1}}{1 - z^{-1}}$$

  $$\frac{V_o(z)}{V_3(z)} = -\frac{C_3}{C_A} \frac{1}{1 - z^{-1}}$$

- For the input $V_1(z)$, the input-output relationship is simply an inverting gain stage, with the input being sampled at the end of $\phi_1$

  $$\frac{V_o(z)}{V_1(z)} = -\frac{C_1}{C_A}$$

- Therefore:

  $$V_o(z) = -\frac{C_1}{C_A} V_1(z) + \frac{C_2}{C_A} \frac{z^{-1}}{1 - z^{-1}} V_2(z) - \frac{C_3}{C_A} \frac{1}{1 - z^{-1}} V_3(z)$$

  $$V_o(z) = -\frac{C_1}{C_A} V_1(z) + \frac{C_2}{C_A} \frac{1}{1 - z} V_2(z) - \frac{C_3}{C_A} \frac{z}{z - 1} V_3(z)$$
Signal Flow Graph Analysis

- In a flow graph the Opamp is separated from the inputs.
- Opamp is represented by: \( \frac{1}{C_A} \frac{1}{1-z^{-1}} \)

- Non-switched capacitor input is represented by a gain of: \( -C_1(1 - z^{-1}) \)
- Delaying switched capacitor is represented by a gain of: \( C_2 z^{-1} \)
- Non-delaying switched capacitor is represented by a gain of: \( -C_3 \)
Example First Order Filter

- Consider a general first order filter

- Start with an active-RC structure and replace resistors with SC equivalents
- Analyse using discrete-time analysis
Example First Order Filter

- Applying the flow chart rules
Example First Order Filter

- Transfer function can easily be derived

\[ C_A(1 - z^{-1})V_o(z) = -C_3 V_o(z) - C_2 V_i(z) - C_1(1 - z^{-1})V_i(z) \]

\[ H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{\left(\frac{C_1}{C_A}\right)(1 - z^{-1}) + \left(\frac{C_2}{C_A}\right)}{1 - z^{-1} + \frac{C_3}{C_A}} \]

\[ = -\frac{\left(\frac{C_1 + C_2}{C_A}\right)z - \frac{C_1}{C_A}}{\left(1 + \frac{C_3}{C_A}\right)z - 1} \]
Example First Order Filter

- Find the pole of the transfer function by equating the denominator to zero:

\[ z_p = \frac{C_A}{C_A + C_3} \]

  - For positive capacitance values, \( z_p \) is restricted to the real axis between 0 and 1 → circuit is always stable

- The zero is found by equating the numerator to zero to yield:

\[ z_z = \frac{C_1}{C_1 + C_2} \]

  - Also restricted to real axis between 0 and 1

- The DC gain found evaluating the transfer function at \( z=1 \):

\[ H(1) = \frac{-C_2}{C_3} \]
Numerical Example: First Order Filter

- Find the capacitance values needed for a first-order SC-circuit such that its 3dB point is at 10kHz when a clock frequency of 100kHz is used.
  - It is also desired that the filter have zero gain at 50kHz (i.e. \( z=-1 \)) and the DC gain be unity
  - Assume \( C_A=10\)pF

Solution:
- Making use of the bilinear transform \( p = \frac{z-1}{z+1} \) the zero at -1 is mapped to \( \Omega=\infty \)
- The frequency warping maps the -3dB frequency of 10kHz (or \( 0.2\pi \) rad/sample) to:
  \[
  \Omega = \tan\left(\frac{0.2\pi}{2}\right) = 0.3249
  \]
- in the continuous-time domain leading to the continuous-time pole, \( p_p \), required being: \( p_p=-0.3249 \)
Numerical Example: First Order Filter

- This pole is mapped back to $z_p$ given by:
  \[ z_p = \frac{1 + p_p}{1 - p_p} = 0.5095 \]

- Therefore, the transfer function $H(z)$ is given by:
  \[ H(z) = \frac{k(z + 1)}{z - 0.5095} \]

  where $k$ is determined by setting the DC gain to one (i.e. $H(1)=1$) resulting in:
  \[ H(z) = \frac{0.24525(z + 1)}{z - 0.5095} \quad \text{or} \quad H(z) = \frac{0.4814z + 0.4814}{1.9627z - 1} \]

- Equating the these coefficients with the general first order filter transfer function (and assuming $C_A=10\text{pF}$):
  \[ C_1=4.814\text{pF}; C_2=-9.628\text{pF}; C_3=9.628\text{pF} \]
  - The negative capacitance can realised by using a differential input
Switch Sharing

- Some switches of the first order SC circuit are redundant
- Switches that are always connected to the same potential can be shared
  - The top plate of $C_2$ and $C_3$ are always switched to virtual Ground of the Opamp and physical Ground at the same time.
  - Therefore one pair of these switches can be eliminated
Fully Differential Filters

- Most modern SC filters are fully-differential
- Difference between two voltages represents signal (balanced around a common-mode voltage)
- Common-mode noise, drift, etc. is rejected
- Even order distortion terms cancel

\[ v_{p1} = k_1 v_1 + k_2 v_1^2 + k_3 v_1^3 + k_4 v_1^4 + \ldots \]

\[ v_{n1} = -k_1 v_1 + k_2 v_1^2 - k_3 v_1^3 + k_4 v_1^4 + \ldots \]

\[ v_{\text{diff}} = 2k_1 v_1 + 2k_3 v_1^3 + 2k_5 v_1^5 + \ldots \]
Fully Differential Filters

- Fully differential first order filter
  - Two identical copies of the single-ended version
Fully Differential Filters

- Negative continuous-time input: equivalent to a negative $C_1$
Fully Differential Filters

- Note that fully-differential version is essentially two copies of single-ended version, however ... area penalty not twice
- Only one opamp needed (though common-mode circuit also needed)
- Input and output signal swings have been doubled so that same dynamic range can be achieved with half capacitor sizes (from $kt/C$ analysis)
- Switches can be reduced in size since small caps used
- However, there is more wiring in fully-differ version but better noise and distortion performance
Low-Q Biquad Filter

- Higher order filters require biquadratic transfer functions

\[ H_a(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{k_2 s^2 + k_1 s + k_o}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \]

- Using flow chart analysis, one can obtain:
Low-Q Biquad Filter

- Implemented as a SC:
Low-Q Biquad Filter

- Flow chart representation:

\[ H(z) = \frac{V_{o}(z)}{V_{i}(z)} = \frac{(K_{2} + K_{3})z^{2} + (K_{1}K_{5} - K_{2} - 2K_{3})z + K_{3}}{(1 + K_{6})z^{2} + (K_{4}K_{5} - K_{6} - 2)z + 1} \]
The individual coefficients of “z” can be equated by comparing to the transfer function

\[ H(z) = \frac{-a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + 1} \]

- \( K_3 = a_0 \)
- \( K_2 = a_2 - a_0 \)
- \( K_1 K_5 = a_0 + a_1 + a_2 \)
- \( K_6 = b_2 - 1 \)
- \( K_4 K_5 = b_1 + b_2 + 1 \)

A degree of freedom is available here in setting internal \( V_1(z) \) output
Low-Q Biquad Filter Design

- Can do proper dynamic range scaling
- Or let the time-constants of 2 integrators be equal by:

\[ K_4 = K_5 = \sqrt{b_1 + b_2 + 1} \]

- Low-Q Biquad Capacitance Ratio
- Comparing resistor circuit to SC circuit, we have

\[ K_4 \approx K_5 \approx \omega_0 T \]
\[ K_6 \approx \frac{\omega_0 T}{Q} \]

- However, the sampling-rate, \(1/T\), is typically much larger than the approximated pole-frequency \(\omega_0\), so \(\omega_0 T \ll 1\)
Low-Q Biquad Capacitance Ratio

- Thus, the largest capacitors determining pole positions are the integrating capacitors $C_1$ and $C_2$
- If $Q<1$, the smallest capacitors are $K_4C_1$ and $K_5C_2$ resulting in an approximate capacitance spread of $1/ (\omega_0 T)$
- If $Q<1$, then the smallest capacitor would be $K_6C_2$ resulting in an approximate capacitance spread of $Q/(\omega_0 T)$
  - can be quite large for $Q>>1$
    - due to a large damping resistor $Q/ \omega_0$
- Use a high-Q biquad filter circuit when for $Q \gg 1$
- $Q$-damping done with a cap around both integrators
- Alternative active-RC prototype filter:
- SC implementation
- Q-damping now performed by $K_6C_1$
High-Q Biquad

- Input $K_1 C_1$: major path for lowpass
- Input $K_2 C_1$: major path for band-pass filters
- Input $K_3 C_2$: major path for high-pass filters
- General transfer function is:

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{K_3 z^2 + (K_1 K_5 + K_2 K_5 - 2K_3)z + (K_3 - K_2 K_5)}{z^2 + (K_4 K_5 + K_5 K_6 - 2)z + (1 - K_5 K_6)}$$

- If matched to the following general form:

$$H(z) = \frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$$

$$K_1 K_5 = a_0 + a_1 + a_2$$
$$K_2 K_5 = a_2 - a_0$$
$$K_3 = a_2$$
$$K_4 K_5 = 1 + b_0 + b_1$$
$$K_5 K_6 = 1 - b_0$$

- Freedom to determine the coefficients
  - Reasonable choice is:

$$K_4 = K_5 = \sqrt{1 + b_0 + b_1}$$
Charge Injection

- To reduce charge injection (thereby improving distortion), turn off certain switches first.
- Advance $\phi_{1a}$ and $\phi_{2a}$ so that only their charge injection affect circuit. The result is a dc offset.
Charge Injection

- Note: $\phi_{2a}$ connected to ground $\phi_{1a}$ while connected to virtual ground, therefore:
  - can use single n-channel transistors
  - charge injection NOT signal dependent

$$Q_{CH} = -WLC_{ox}V_{eff} = -WLC_{ox}(V_{GS} - V_t)$$

- Charge related to $V_{GS}$ and $V_t$
  - $V_t$ related to substrate-source voltage, thus $V_t$ remains constant
- Source of $Q_3$ and $Q_4$ remains at 0 volts $\rightarrow$ amount of charge injected by $Q_3, Q_4$ is not signal dependent and can be considered as a DC offset
Charge Injection Example

- Estimate DC offset due to channel-charge injection when $C1=0$ and $C2 = C4 = 10C3 = 10pF$
- Assume switches $Q_3$, $Q_4$ have $V_t=0.8V$, $W=30\mu m$, $L=0.8\mu m$ and $C_{ox}=1.9e-3$ pF/mm$^2$, and power supplies are $\pm2.5V$

**Solution:**
- Channel charge of $Q3$, $Q4$ (when on ) is:

\[
Q_{CH3} = Q_{CH4} = -(30)(0.8)(0.0019)(2.5 - 0.8) \\
= -77.5 \times 10^{-3} \ pC
\]
- DC feedback keeps Opamp input at virtual ground (0V)
Charge Injection Example

Charge transfer into given by:

\[ Q_{C3} = -C_3 v_{out} \]

We estimate half channel-charges of \( Q_3, Q_4 \), are injected to the virtual ground leading to:

\[ \frac{1}{2}(Q_{CH3} + Q_{CH4}) = Q_{C3} \]

Thus:

\[ v_{out} = \frac{77.5 \times 10^{-3}}{1 \text{pF}} \text{ pC} = 78 \text{ mV} \]

DC offset affected by the capacitor sizes, switch sizes and power supply voltage
SC Gain Circuits – Parallel RC

- SC circuits can be used for signal amplification
- General Gain circuit with two parallel RC:

\[ v_{out}(t) = -Kv_{in}(t) \]

- SC implementation:
  - circuit amplifies 1/f noise as well as Opamp offset
SC Gain Circuits

- Resettable Gain Circuit
  - Resets integrating capacitor $C_2$ every clock cycle
  - Performs offset cancellation
  - Also highpass filters $1/f$ noise of Opamp
  - However, requires a high slew-rate from Opamp

\[
y_{out}(n) = -\left(\frac{C_1}{C_2}\right)y_{in}(n)
\]
SC Gain Circuits

- Resettable Gain Circuit
- Offset cancellation

\[ v_{out}(n) = -\left(\frac{C_1}{C_2}\right)v_{in}(n) \]
SC Gain Circuits

- Capacitive Reset
- Eliminate slew problem and still cancel offset by coupling Opamp’s output to inverting input
- $C_4$ is optional de-glitching capacitor

$$v_{out}(n) = -\left(\frac{C_1}{C_2}\right)v_{in}(n)$$
SC Gain Circuits

- Capacitive Reset
- During Reset
- During valid output
SC Gain Circuits

- Differential Capacitive Reset

- Accepts differential inputs and partially cancels switch clock-feedthrough

\[ v_{out} = \left( \frac{C_1}{C_2} \right) (v_{in}^+ - v_{in}^-) \]
Correlated Double Sampling (CDS)

- Preceding SC gain circuit is an example of CDS
  - Minimizes errors due to Opamp offset and 1/f noise
- When CDS used, Opamps should have low thermal noise (often use n-channel input transistors)
- Often use CDS in only a few stages:
  - input stage for oversampling converter
  - some stages in a filter (where low-frequency gain is high)
- Basic approach:
  - Calibration phase: store input offset voltage
  - Operation phase: error subtracted from signal
Better High-Freq CDS Amplifier

- $\phi_2: \ C_1', C_2'$ used but include errors
- $\phi_1: \ C_1', C_2'$ used but here no offset errors
CDS Integrator

- $\phi_1$: sample offset on $C_2$
- $\phi_2$: $C_2$ placed in series with Opamp to reduce error
- Offset errors reduced by Opamp gain
- Can also apply this technique to gain amps
SC Amplitude Modulator

- Square wave modulate by ±1 (i.e. $V_{out} = \pm V_{in}$)
- Makes use of cap-reset gain circuit
- $\phi_{ca}$: is the modulating signal
SC Full-Wave Rectifier

- Use square wave modulator and comparator to make
- For proper operation, comparator output should change synchronously with the sampling instances
SC Peak Detector

- Left circuit can be fast but less accurate
- Right circuit is more accurate due to feedback but slower due to need for compensation
  - circuit might also slew so Opamp’s output should be clamped